100V Half-Bridge GaN Driver with Tri-State PWM Input

1. Features

- Single Tri-State PWM Input
- Split Outputs for Adjustable Turn-on/-off Speeds
- Strong 1-Ω Pull-Up and 0.2-Ω Pull-Down Resistance
- Internal Strong and Smart Bootstrap Switch
- Adjustable Dead Time Optimized for GaN FETs
- Adaptive Shoot-Through Protection
- Fast Propagation Delay (22ns Typical)
- High-Side Floating Supply Operates up to 100V
- Built-In UVLO, OVLO, OTP Protections
- FCQFN 3mmx3mm Package

2. Applications

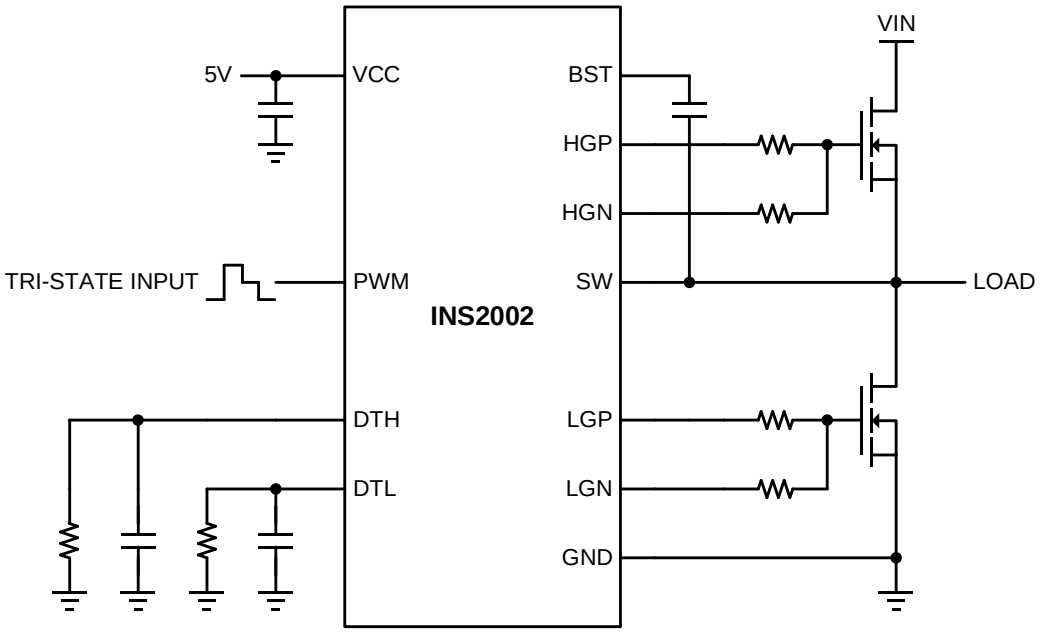
- Half-Bridge and Full-Bridge Converters
- High-Voltage Synchronous DC-DC Converters
- High Frequency, High Power Density Applications
- 48V DC Motor Drive
- High Power Class-D Audio Power Amplifier
- Automotive 48V/12V Bi-directional DC-DC

3. Description

The INS2002 is a 100V half-bridge driver designed for efficient driving of gallium nitride (GaN) field-effect transistors (FETs), customized to address challenges commonly encountered in conventional MOSFET drivers. It includes an internal smart bootstrap (BST) switch to prevent overcharging of the high-side driver supply during dead times, protecting the gate of the GaN FET while maintaining consistent gate voltage for both drivers. The INS2002 optimizes gate switching timing by monitoring true gate voltages to achieve near-zero dead time, enhancing efficiency and enabling high-frequency operation. Alternatively, Users can adjust dead times using external resistors for specific application needs.

The INS2002 features a tri-state PWM input, allowing it to be driven high, low, or left floating for both sides of switches off. Additionally, it offers split outputs to independently adjust turn-on and turn-off speeds. Its strong driving capability and fast propagation delay make the INS2002 suitable for high-power and high-frequency applications.

4. Typical Application



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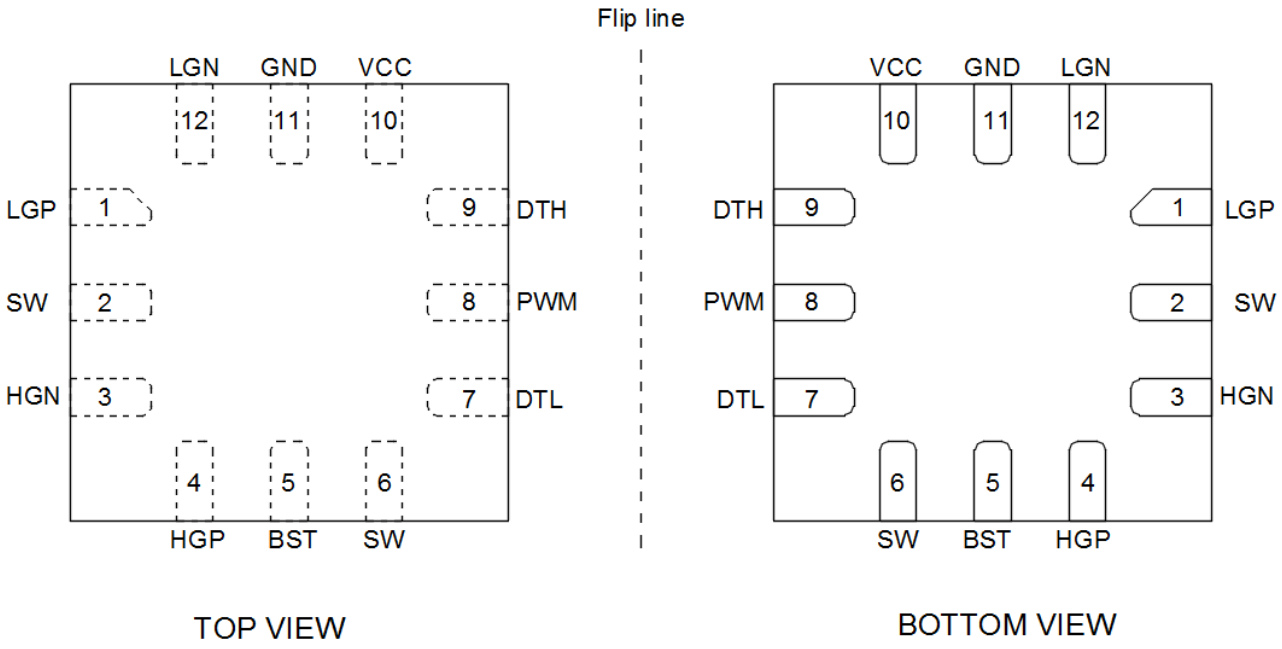
5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-07-30	Final datasheet release

6. Pin Configuration and Functions



12-Lead FCQFN (3mm x 3mm) Package

Pin Number	Pin Name	Description
1	LGP	Low-Side Gate Driver Pull-Up Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-on speed.
2, 6	SW	Switch Node. Connect to the negative terminal of the bootstrap capacitor, the source of the high-side GaN FET, and the drain of the low-side GaN FET.
3	HGN	High-Side Gate Driver Pull-Down Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-off speed.
4	HGP	High-Side Gate Driver Pull-Up Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-on speed.
5	BST	High-Side Gate Driver Bootstrap Supply. Locally bypass this pin to SW with a ceramic bootstrap capacitor.
7	DTL	Dead Time Setting for High-to-Low Transition. Connect a resistor to GND.
8	PWM	PWM Input. This pin receives tri-state input and controls the driver outputs.
9	DTH	Dead Time Setting for Low-to-High Transition. Connect a resistor to GND.
10	VCC	IC and Low-Side Gate Driver Supply. Locally bypass this pin to GND with a ceramic capacitor.
11	GND	Ground. All signals are referenced to this ground.
12	LGN	Low-Side Gate Driver Pull-Down Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-off speed.

7. Absolute Maximum Ratings

All pins are referred to GND, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device reliability and lifetime.

Parameter	Min	Max	Unit
VCC	-0.3	6	V
BST to SW	-0.3	6	V
PWM, DTH, DTL	-0.3	6	V
HGP, HGN	SW-0.3	BST+0.3	V
LGP, LGN	-0.3	VCC+0.3	V
SW	-5	100	V
BST	-0.3	105	V
Operating Junction Temperature T_J	-40	150	˚C
Storage Temperature	-55	150	˚C

8. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002	±1000	V

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
VCC	4.5	5.5	V
PWM	0	5.5	V
SW	-4	80	V
BST	SW+4.5	SW+5.5	V
SW Slew Rate		50	V/ns
Operating Junction Temperature T_J	-40	125	˚C

10. Thermal Information

Symbol	Parameter	INS2002FQ	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	68.82	˚C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top)	59.65	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	16.94	˚C/W

11. Electrical Characteristics

T_J = 25°C, VCC = BST = 5V, SW = GND = 0V, HGP = HGN = HG, LGP = LGN = LG, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Input						
VCC quiescent current	I_{CC-Q}		360	600	μA	PWM = High-Z, R_{DTH}=R_{DTL}=75kΩ
VCC operating current	I_{CC-OP}		1.5	3	mA	f = 500kHz
BST quiescent current	I_{BST-Q}		40	70	μA	PWM = High-Z
BST operating current	I_{BST-OP}		1.5	3	mA	f = 500kHz
VCC overvoltage rising threshold	V_{CC-OVR}	5.7	6	6.3	V	
VCC overvoltage hysteresis	$V_{CC-OVHYS}$		0.25		V	
VCC undervoltage rising threshold	V_{CC-UVR}	3.9	4.1	4.3	V	
VCC undervoltage hysteresis	$V_{CC-UVHYS}$		0.3		V	
BST undervoltage rising threshold	$V_{BST-UVR}$		3.6		V	
BST undervoltage hysteresis	$V_{BST-UVHYS}$		0.5		V	
PWM Input						
Input high threshold	V_{IH}	2	2.2	2.4	V	PWM rising
Input high hysteresis	V_{IH-HYS}	0.1	0.2	0.3	V	
Input low threshold	V_{IL}	0.8	1	1.2	V	PWM falling
Input low hysteresis	V_{IL-HYS}	0.1	0.2	0.3	V	
Input tri-state float voltage	V_{TRI}	1.4	1.6	1.8	V	
Internal pull-up resistor	R_{IUP}		10		kΩ	To internal 3.2V supply
Internal pull-down resistor	R_{IDN}		10		kΩ	
Bootstrap Switch						
Low-current forward voltage			0.02	0.2	V	$I_{VCC-BST}$ = 100μA
High-current forward voltage			0.4		V	$I_{VCC-BST}$ = 100mA
Switch on resistance	$R_{BST(ON)}$		4		Ω	
High-Side and Low-Side Gate Driver						
Output pull-down resistance	R_{DN}		0.2	1	Ω	I_{HGN} or I_{LGN} = 100mA
Output pull-up resistance	R_{UP}		1	2	Ω	I_{HGP} or I_{LGP} = -100mA
Output peak source current(1)	I_{OH}		1.7		A	HG = SW or LG = GND
Output peak sink current(1)	I_{OL}		4.3		A	HG = BST or LG = VCC
Dead time pin voltage	V_{DT}		1.21		V	
Over Temperature Protection						
OTP shutdown rising threshold(1)	T_{OTP}		165		°C	
OTP shutdown hysteresis(1)	$T_{OTP-HYS}$		20		°C	

12. Switching Characteristics

T_J = 25°C, VCC = BST = 5V, SW = GND = 0V, HGP = HGN = HG, LGP = LGN = LG, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum input pulse width that changes the output (1)	T_{IPW}		5		ns	
Minimum gate output pulse width (1)	T_{OPW}		55		ns	
Gate output rise time (1)	T_R		7		ns	C_L = 1nF, 10% to 90%
Gate output fall time (1)	T_F		3		ns	C_L = 1nF, 90% to 10%
Dead time – LG off to HG on (1)	T_{DTH}		2 15		ns ns	R_{DTH} = 36kΩ R_{DTH} = 270kΩ
Dead time – HG off to LG on (1)	T_{DTL}		2 15		ns ns	R_{DTL} = 36kΩ R_{DTL} = 270kΩ
High-side turn-off propagation delay (1)	T_{HPHL}		22		ns	PWM falling to HG falling
Low-side turn-off propagation delay (1)	T_{LPHL}		22		ns	PWM rising to LG falling

(1) Not 100% tested and guaranteed by design.

13. Typical Characteristics

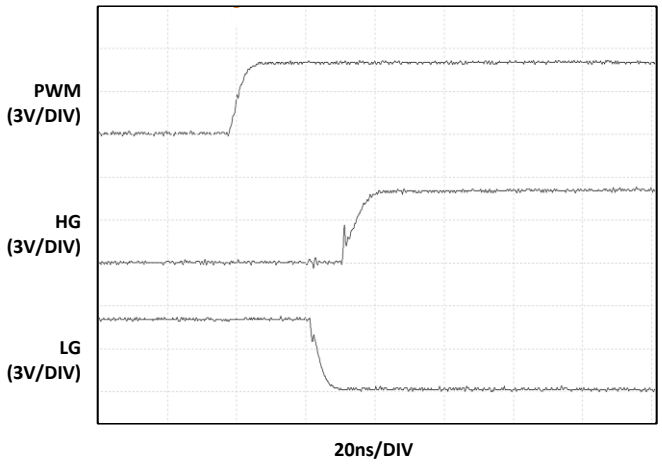


Figure 1. HG On and LG Off, C_{OUT}=1nF, R_{DTH}=R_{DTL}=180kΩ

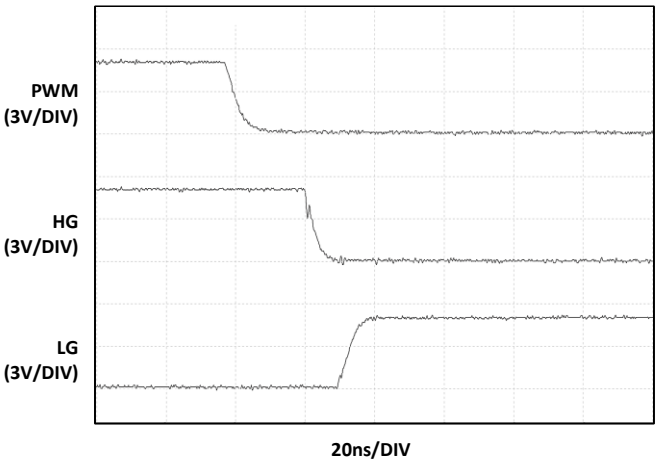


Figure 2. HG Off and LG On, C_{OUT}=1nF, R_{DTH}=R_{DTL}=180kΩ

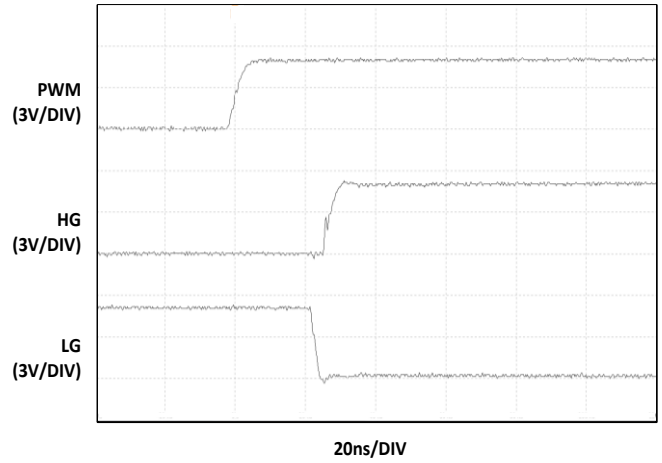


Figure 3. HG On and LG Off, C_{OUT}=470pF, R_{DTH}=R_{DTL}=0kΩ

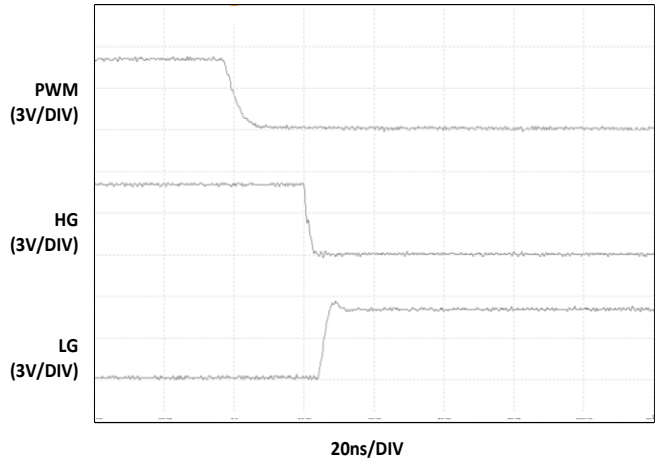


Figure 4. HG Off and LG On, C_{OUT}=470F, R_{DTH}=R_{DTL}=0kΩ

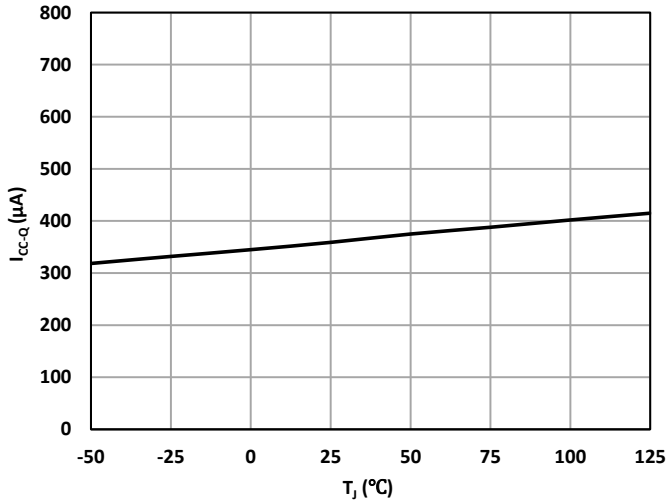


Figure 5. VCC Quiescent Current vs Temperature

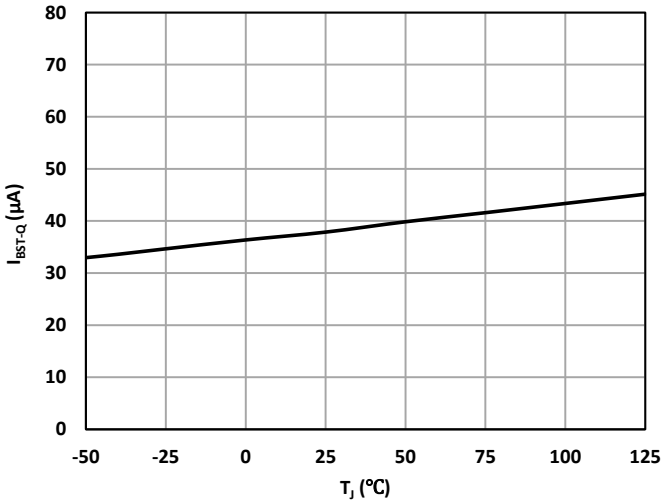


Figure 6. BST Quiescent Current vs Temperature

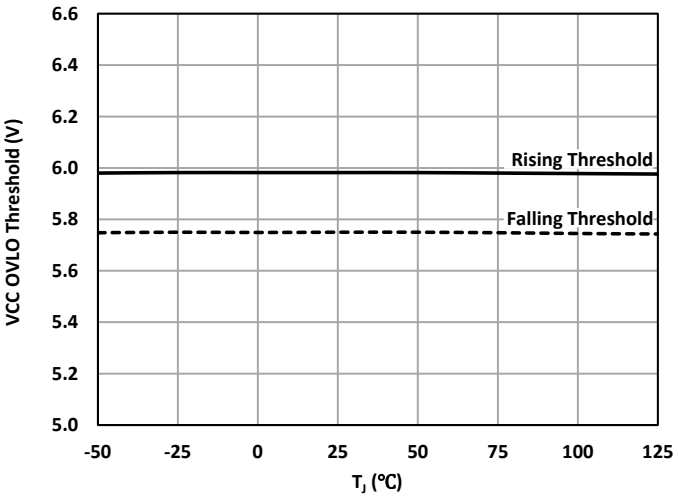


Figure 7. VCC OVLO Threshold vs Temperature

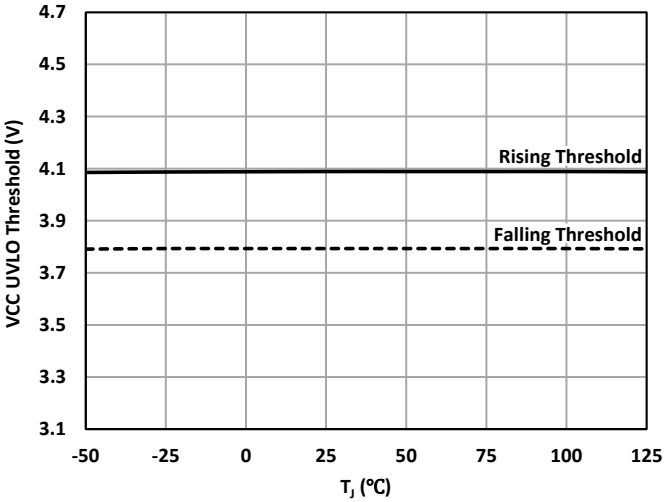


Figure 8. VCC UVLO Threshold vs Temperature

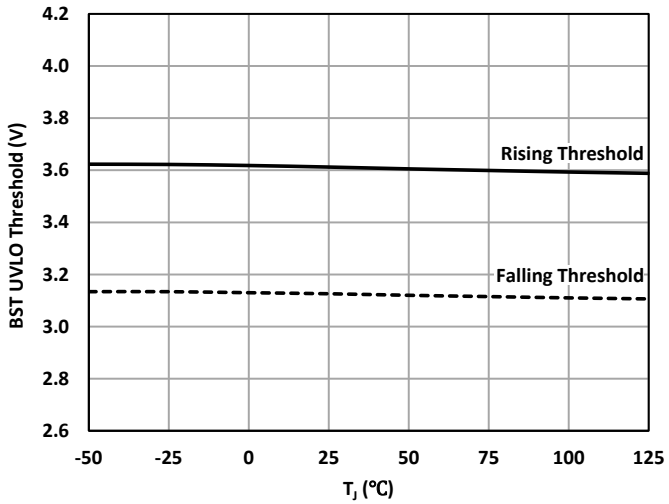


Figure 9. BST UVLO Threshold vs Temperature

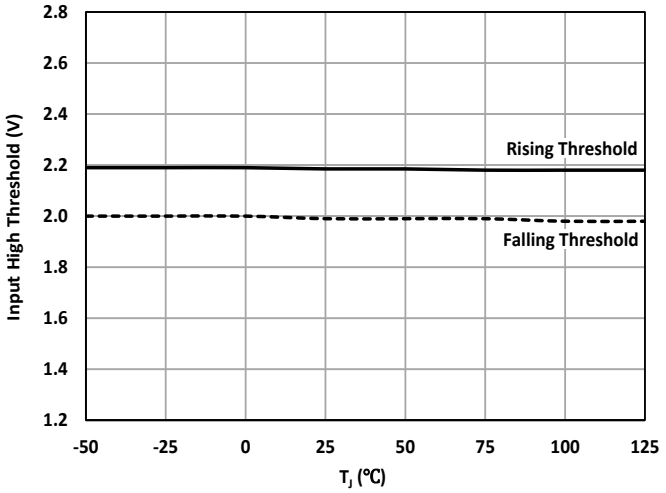


Figure 10. Input High Threshold vs Temperature

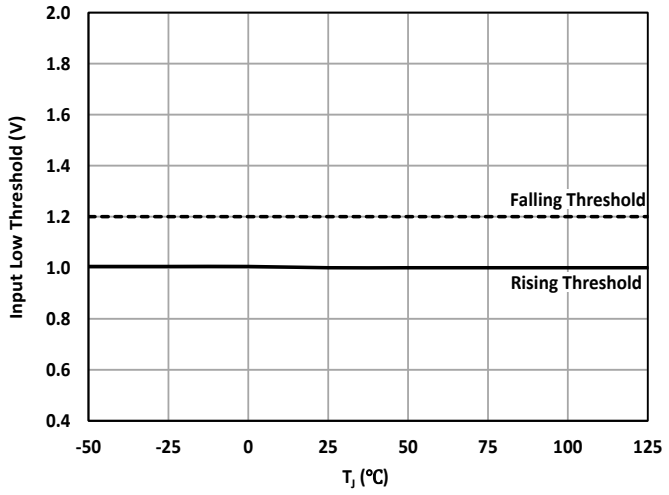


Figure 11. Input Low Threshold vs Temperature

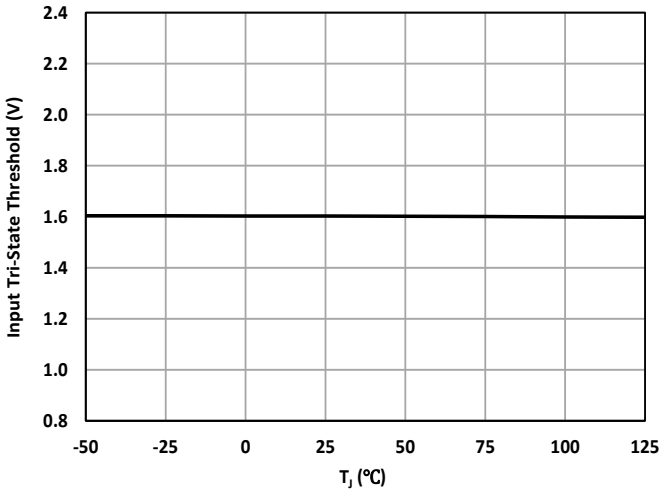


Figure 12. Input Tri-State Float Voltage vs Temperature

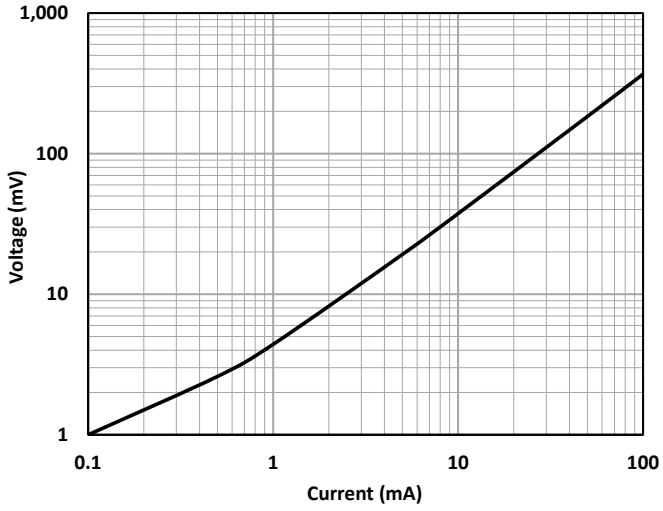


Figure 13. Bootstrap Forward Voltage vs Current

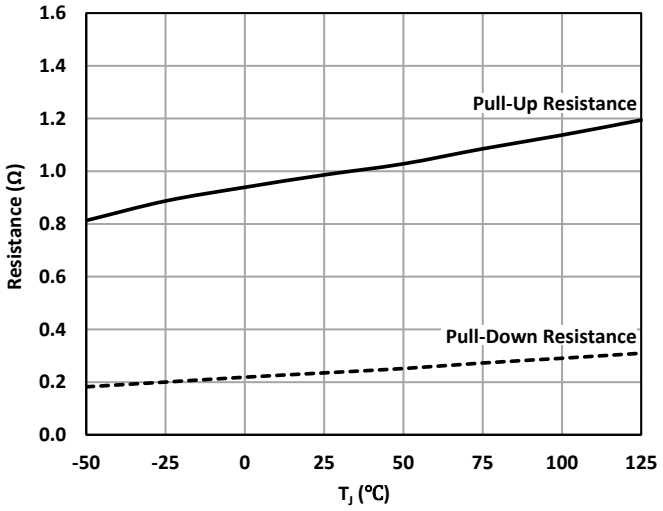


Figure 14. Output Pull-Down/Pull-Up Resistance vs Temperature

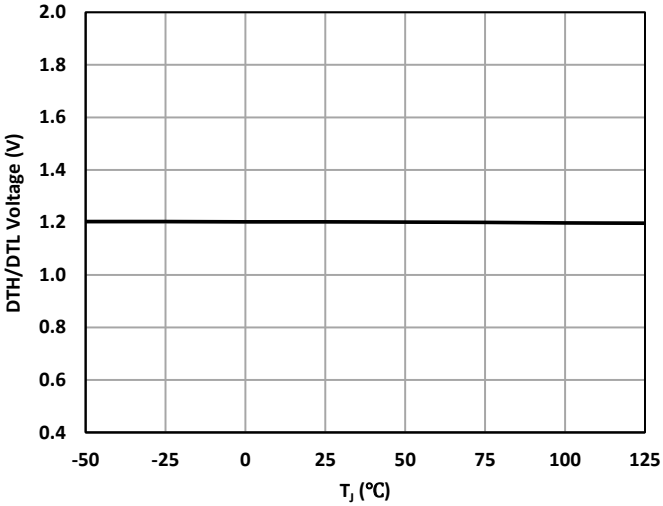


Figure 15. DTH and DTL Voltages vs Temperature

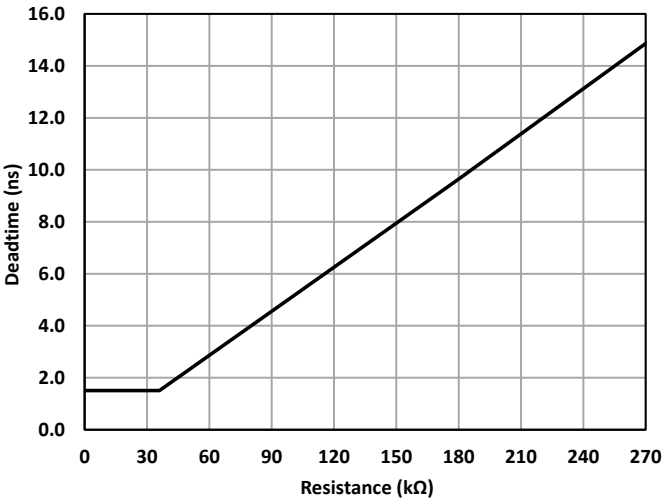


Figure 16. Deadtime vs Resistor Value

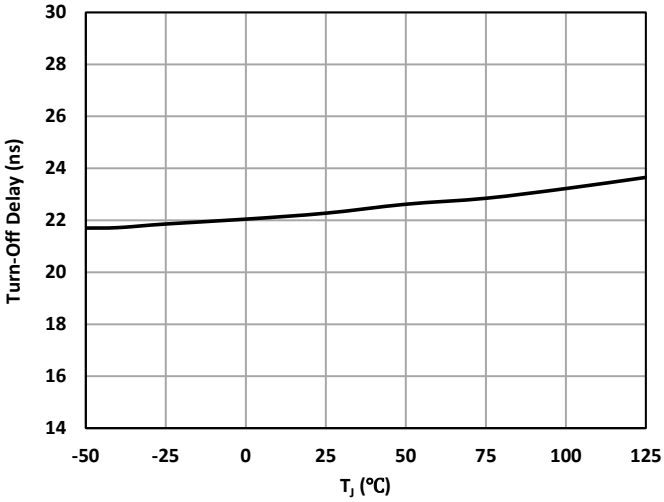


Figure 17. Low-Side Propagation Delay vs Temperature

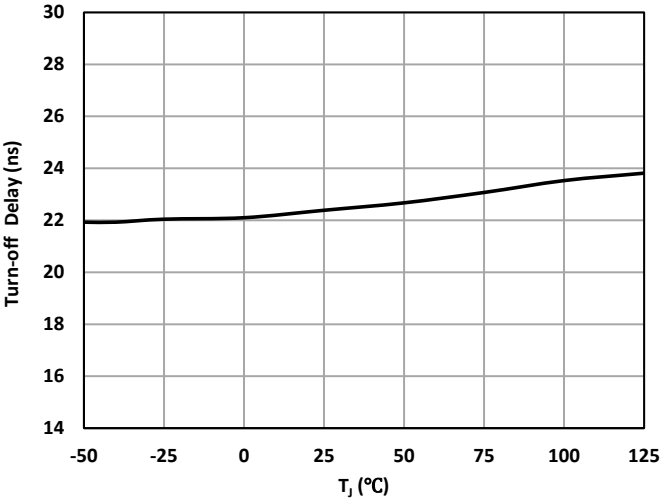


Figure 18. High-Side Propagation Delay vs Temperature

14. Block Diagram

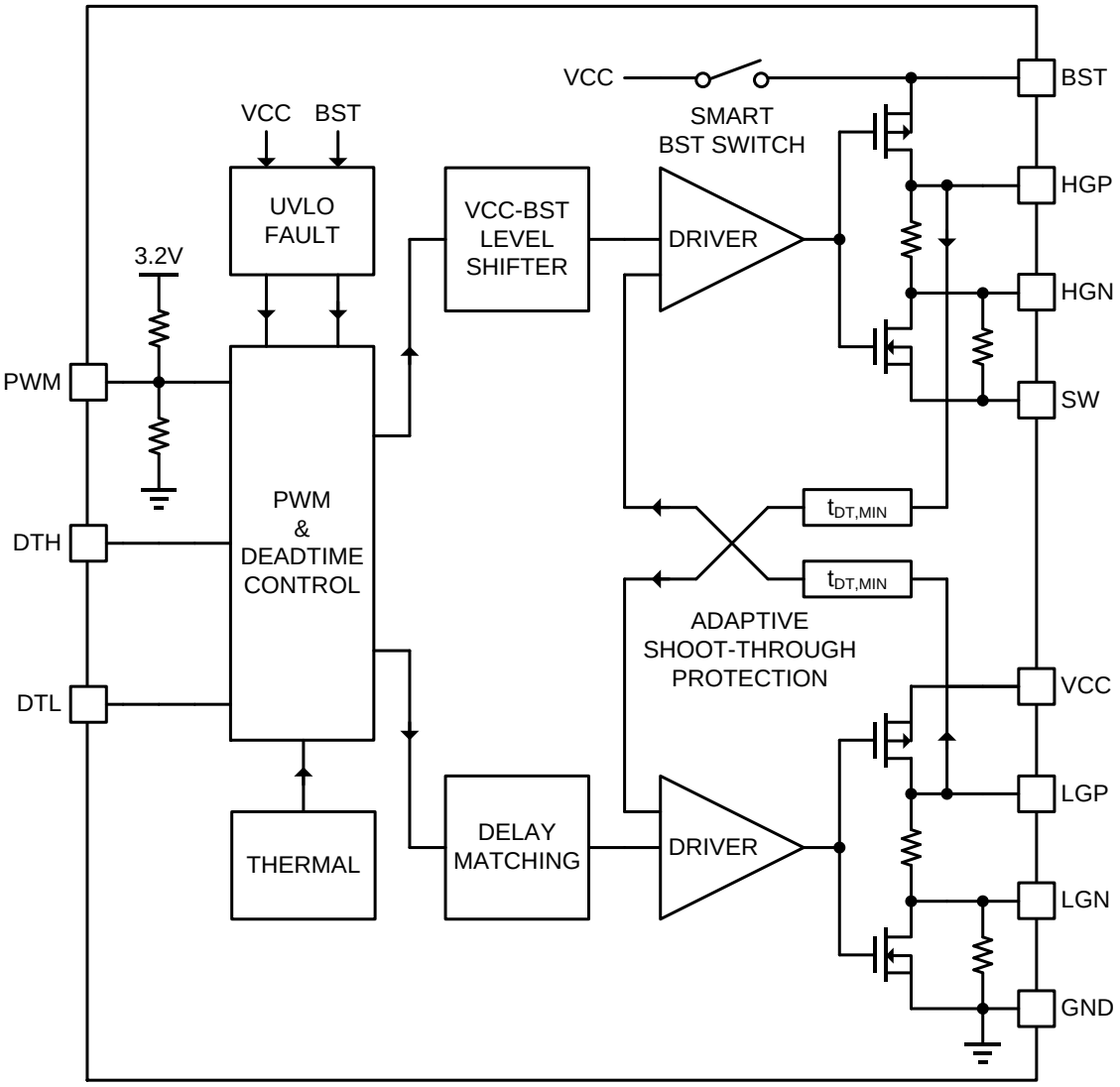


Figure 19. Functional Block Diagram

15. Function Description

The INS2002 is a 100V half-bridge driver optimized for GaN FETs, designed to address the specific challenges encountered when driving GaN FETs with traditional MOSFET drivers. It incorporates an integrated smart BST switch to manage the high-side floating supply so that it charges the BST capacitor to match the VCC supply when the low-side driver turns on. This ensures a consistent gate voltage for both high-side and low-side GaN FETs, preventing overcharging and potential damage to their gates while also ensuring precise delay matching.

The INS2002 achieves near-zero dead time through precise monitoring of true GaN FET gate voltages, enabling efficient high-frequency operation. It also offers programmable dead time up to 15ns for margin or application-specific customization. The INS2002 also provides split gate driver outputs, enabling the independent adjustment of turn-on and turn-off slew rates of both high-side and low-side drivers by connecting different gate resistors. With its strong driving capability and fast propagation delay, the INS2002 is highly suitable for supporting multiple topologies, including buck, boost, buck-boost, and a variety of high-power and high-frequency applications.

Input and Output

The INS2002 employs a tri-state PWM input. The three input states of the INS2002 are depicted in Figure 20. When the input PWM voltage exceeds the input high threshold, V_{IH}, HGP is pulled high and turning on the high-side GaN FET. Similarly, when the input PWM voltage falls below the input low threshold voltage, V_{IL}, LGP is pulled high and turning on the low-side GaN FET. Hysteresis between the corresponding V_{IH} and V_{IL}, denoted as V_{IH_HYS} and V_{IL_HYS} respectively, is provided to eliminate false triggering during the switching transitions caused by noise. If the PWM pin is left float, the INS2002 enters a high-impedance state, and both the high-side and low-side GaN FETs are turned off. During this state, the internal resistor divider sets the PWM pin voltage to 1.6V. The transition thresholds are fixed regardless of VCC voltage. Table 1 summarizes the outputs corresponding to the PWM input state.

The INS2002 features a 5ns (typical) input deglitch filter to remove any unwanted pulses from a PWM input. A narrow input pulse exceeding this deglitch time will be extended to a minimum output pulse of 55ns (typical) to ensure proper gate turn-on and turn-off transients. Additionally, The INS2002 offers fast propagation delay (22ns typical) making it ideal for high-frequency applications. Figure 20 shows the switching characteristics of the input and output.

Table 1. Input and Output Truth Table

PWM	HGP	HGN	LGP	LGN
L	Open	L	H	Open
H	H	Open	Open	L
Hi-Z	Open	L	Open	L

Note: When an output is “Open”, it is connected to another split output through the internal 10kΩ resistor.

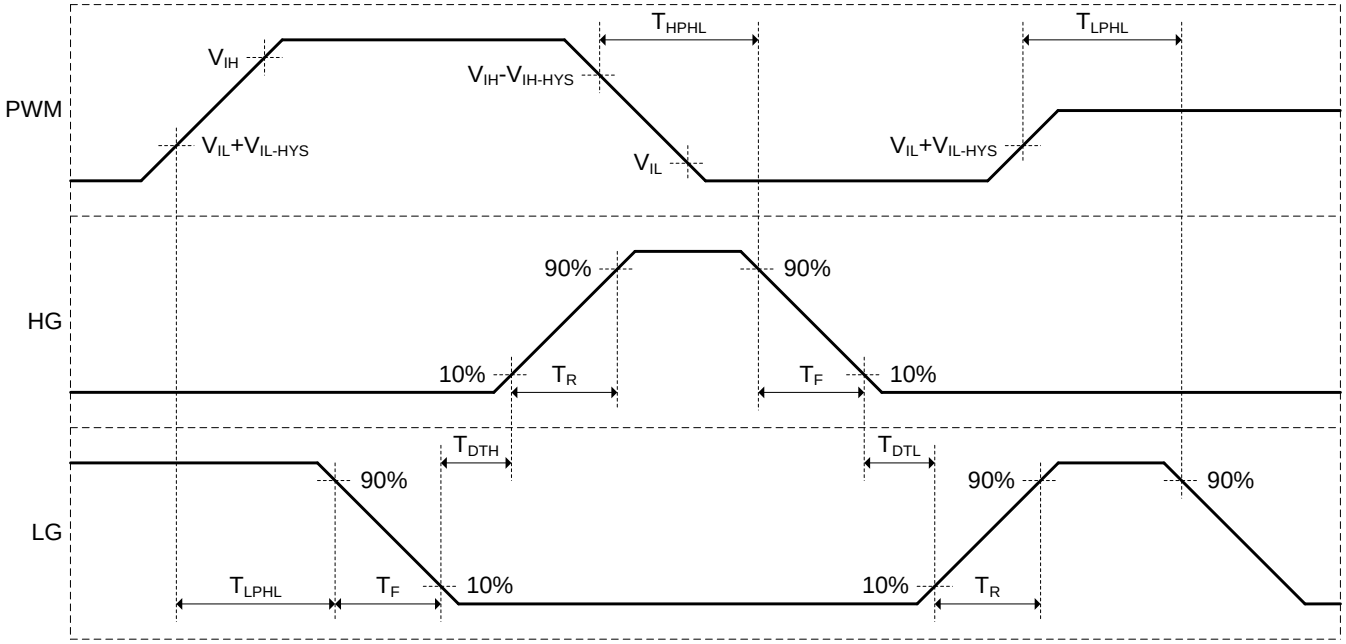


Figure 20. Timing Diagram of Input and Output

Split Gate Driving Output

The INS2002 provides split gate driver outputs for both high-side and low-side GaN FETs, offering flexibility to adjust both turn-on and turn-off strengths independently. This is achieved by connecting additional gate resistors at HGP, HGN, LGP, and LGN pins, targeting optimization of efficiency, reliability, and EMI performance. The strong pull-down and pull-up gate strength of the INS2002 are optimized for driving GaN FETs, enabling high-frequency and high-efficiency operations. With a strong pull-down strength of 0.2Ω (typical) at HGN and LGN pins, it provides a robust low impedance path necessary for eliminating high dv/dt induced gate turn-on. Meanwhile, the pull-up strength of 1Ω (typical) at HGP and LGP pins helps in reducing the switching spikes and overshoot voltages at the switch node. HGN and LGN pins have internal 50kΩ pull-down resistors to SW node and GND nodes, respectively, and are also internally connected to HGP and LGP via 10kΩ resistors, respectively.

VCC UVLO/OVLO Protections

The INS2002 features undervoltage lockout (UVLO) and overvoltage lockout (OVLO) for VCC, providing the operation under the safe conditions of devices. When the VCC voltage falls below its UVLO threshold of 3.8V (typical) or exceeds above its OVLO threshold of 6.0V (typical), the INS2002 turns off both the high-side and low-side drivers and ignores the PWM input.

High dv/dt Rate GaN FET Switching

GaN FETs can switch much faster than traditional silicon based MOSFETs, requiring gate drivers capable of delivering precise and fast switching signals to fully leverage their potential. Managing high dv/dt rates during switching is important for stable gate driver circuitry, ensuring reliable and efficient operation. The INS2002 features an advanced floating level-shifter circuit designed to overcome these challenges associated with driving GaN FETs. Its advanced noise rejection mechanism ensures precise and accurate signal transmission between the control logic to driver outputs even in extreme high dv/dt environments up to 50V/ns.

Another challenge in driving GaN FETs is the issue of high reverse conduction voltage. When the SW node drops below 0V due to this reverse conduction, it can temporarily lower the level shifter's supply rail, causing a disruption in the level

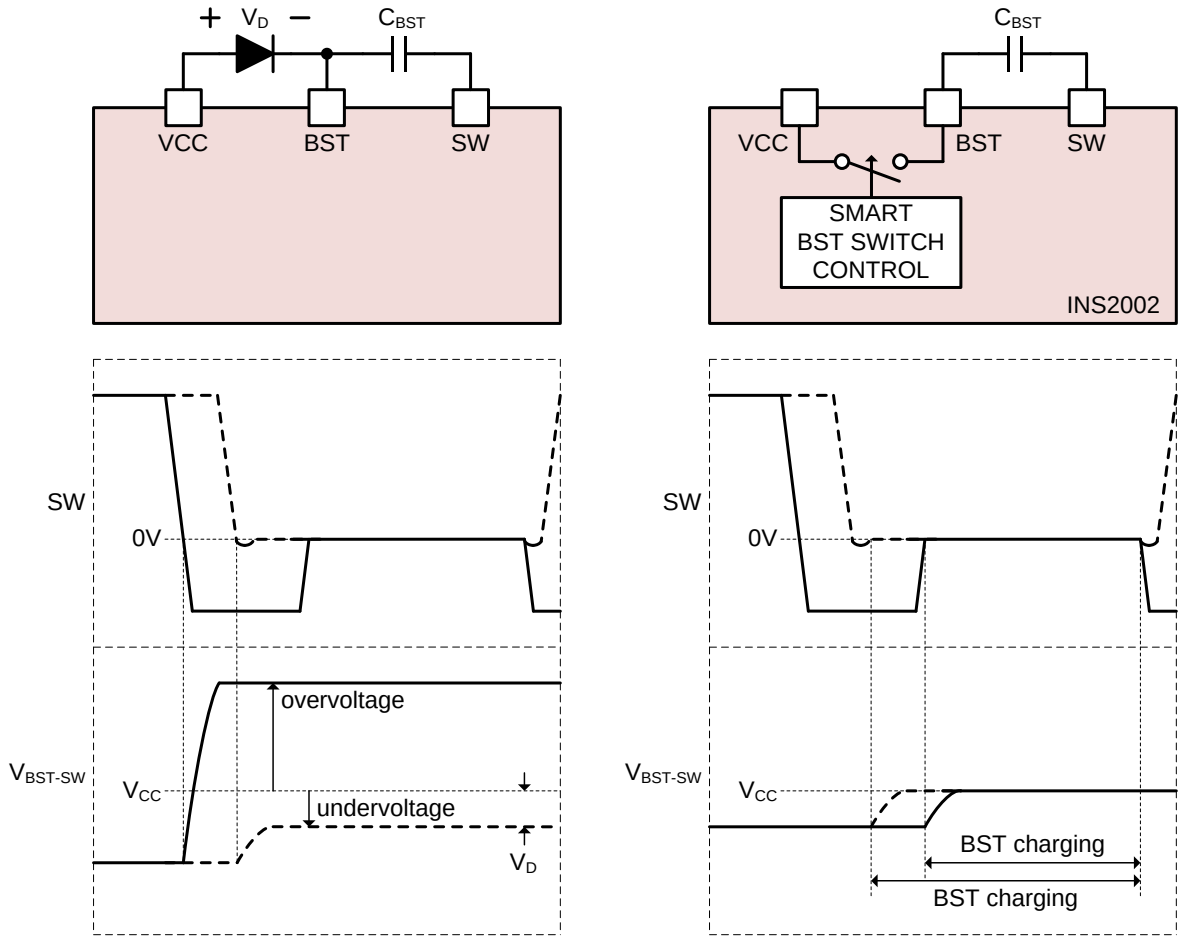
shifter's output signals. This disruption can appear as a delay mismatch between signals transmitted to each side of the driver, resulting in timing inaccuracies and potential performance degradation. The proposed level shifter in the INS2002 is designed to prevent such conditions, ensuring the delay variation is kept to a minimum (1ns typical) even when the SW node fluctuates by up to -4V. Additionally, the INS2002 features an additional delay matching circuit that parallels the proposed level shifter circuit, matching its process and temperature variation characteristic. This additional feature further improves delay matching to 1ns (typical).

High-Side Gate-Driver Supply

Despite GaN devices offering advantages with their superior figure of merit ($Q_G \times R_{DSON}$) compared to silicon based MOSFET counterparts, their sensitivity to gate driving voltage levels presents a challenging concern. GaN devices are more vulnerable to both overvoltage and undervoltage conditions at the gate, which can have negative effects on their reliability and performance. The concern over gate overvoltage is more significant for GaN FETs, given that they are considerably more fragile compared to their silicon counterparts. Conversely, insufficient gate voltage, or gate undervoltage, can result in increased switching losses and reduced efficiency.

To mitigate these challenges, the INS2002 features a smart BST switch that allows precise control for BST charging and blocking. Figure 21 illustrates the operation principle of the smart BST switch. Unlike silicon MOSFETs, GaN FETs typically lack an intrinsic body diode, resulting in higher reverse conduction voltages, (typically 2V to 3V or even higher at high current) during dead time. This can lead to overcharging of the BST capacitor, potentially causing permanent damage to the gate of the high-side GaN FET. In the INS2002, the BST switch's turning on and off are precisely controlled so that it allows charging of the BST capacitor only during SW node is fully reached at GND voltage when the low-side GaN FET is being turned on. Moreover, the BST switch exhibits a low on-impedance of 4Ω (typical), ensuring minimal dropout voltage. Accordingly, the INS2002 always maintains a well-balanced BST rail voltage close to VCC, achieving excellent delay matching and balanced gate driving strength between the high-side and low-side drivers.

Additionally, the INS2002 provides a BST UVLO protection with a falling threshold of 3.1V (typical) and a rising threshold of 3.6V (typical). When BST-SW falls below BST UVLO threshold, the INS2002 enters UVLO mode, turns off the high-side driver, but the low-side driver remains activated.



(a) Conventional Bootstrap Diode (b) Smart Bootstrap Switch

Figure 21. Block and Timing Diagram of Bootstrap Circuit

Dead Time Control

Dead time control is crucial in half-bridge applications for optimizing efficiency and enabling high-frequency operations. The INS2002 allows dead time programming from 15ns to near-zero by configuring the DTH and DTL pins. The DTH pin sets the dead time from the low-side gate (LGN) turning off to the high-side gate (HGP) turning on, while the DTL pin sets the dead time from the high-side gate (HGN) turning off to the low-side gate (LGP) turning on. By default, tying the DTH and/or DTL pins to GND reduces dead time delays to near-zero. The INS2002 features an internal shoot-through protection circuit, leveraging shunt sensing of the true gate voltage of GaN FETs through its split outputs structure. It offers precise switching timing control for immediate turn-on after complete turn-off of the opposite side to ensure that they do not conduct simultaneously in any situation. All this is processed within a nanosecond range to achieve that near-zero dead time delay.

Connecting a resistor, R_{DT}, between DTH and/or DTL and GND sets an additional delay from 1ns to 15ns to the dead time. Choose a R_{DT} value from Equation (1) or Figure 22, as follows:

$$\text{Dead Time}=\max\left(\frac{1\text{ns}}{18\text{k}\Omega}\times R_{DT},1\text{ns}\right) \quad (1)$$

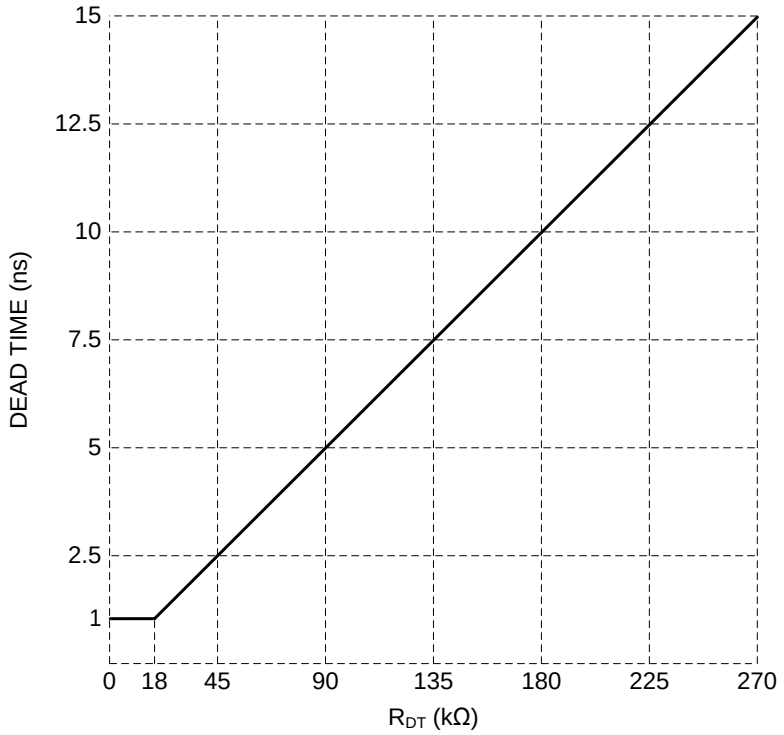


Figure 22. Dead Time vs R_{DT}

Over Temperature Protection (OTP)

The INS2002 employs over temperature protection (OTP). If the internal junction temperature, T_j, exceeds 165°C (typical), The PWM input is ignored, and both the high-side and low-side drivers are turned off. When the temperature drops below 145°C (typical), the INS2002 will resume normal operation.

Layout Recommendation

A proper PCB layout is essential to support high-power and high-frequency operation with GaN FETs. The PCB layout requires proper bypassing on (VCC-GND) and (BST-SW) and careful trace routing to minimize the parasitic of the gate driving and power loops. Check the following guidelines and Figure 23 to obtain the optimum performance from the INS2002.

1. Mount the bypass capacitors for (VCC-GND) and (BST-SW) as close as possible to the INS2002 package. Also place the bypass capacitors on the same side as the INS2002. Carefully implement the power loop to minimize the length of the copper trace.

2. Place the INS2002 as close as possible to the GaN FETs and keep the copper trace between the INS2002 and GaN FETs short and wide.

3. To minimize the gate voltage ringing, it is desirable to place gate resistors close to both the INS2002 and GaN FETs.

4. Place both high-side and low-side GaN FETs close together to minimize the parasitic inductance in between.

5. Place R_{DTH} and R_{DTL} as close to the INS2002 as possible and minimize the signal coupling from noisy signals to DTH and DTL traces. It is recommended to put 50pF capacitors in parallel with R_{DTH} and R_{DTL}.

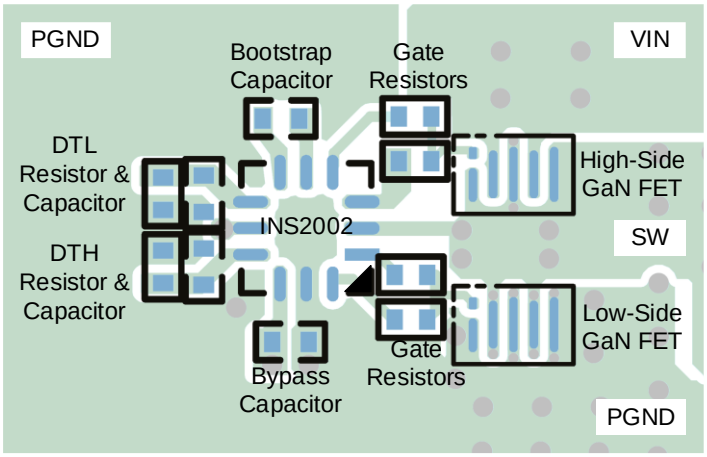
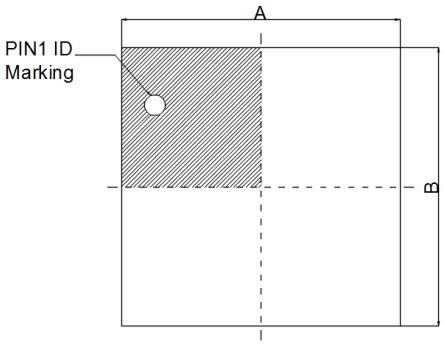


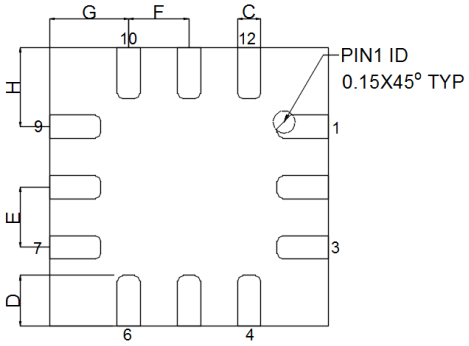
Figure 23. Layout Example

16. Package Information

FCQFN3X3-12L Package:

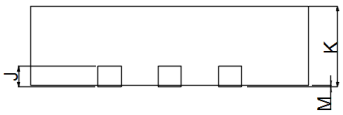


TOP VIEW



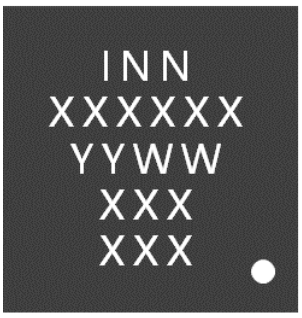
BOTTOM VIEW

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	2.9	3.0	3.1	
B	2.9	3.0	3.1	
C	0.20	0.25	0.30	12X
D	0.45	0.55	0.65	12X
E	0.65 BASIC			4X
F	0.65 BASIC			4X
G	0.85 REF			4X
H	0.85 REF			4X
J	0.203 REF			
K	0.75	0.85	0.95	
M	0.00	0.02	0.05	



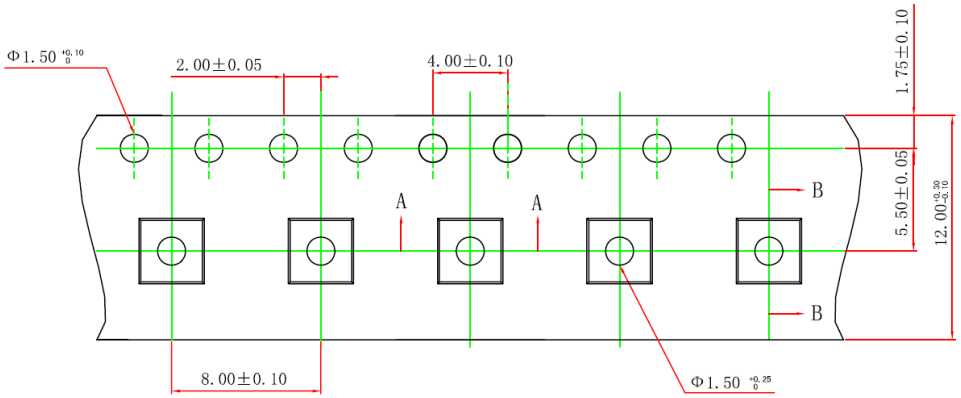
SIDE VIEW

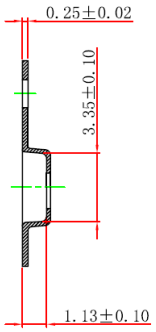
NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS FT TESTER SIDE VIEW.
3)LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-220.
5)DRAWING IS NOT TO SCALE.



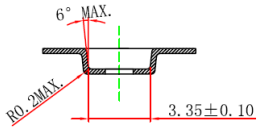
ROW	Description	Example
Row 1	Company Name	INN
Row 2	Product Code	XXXXXX
Row 3	Date Code	YYWW
Row 4	Lot Code	XXX
Row 5		XXX

17. Tape and Reel Information

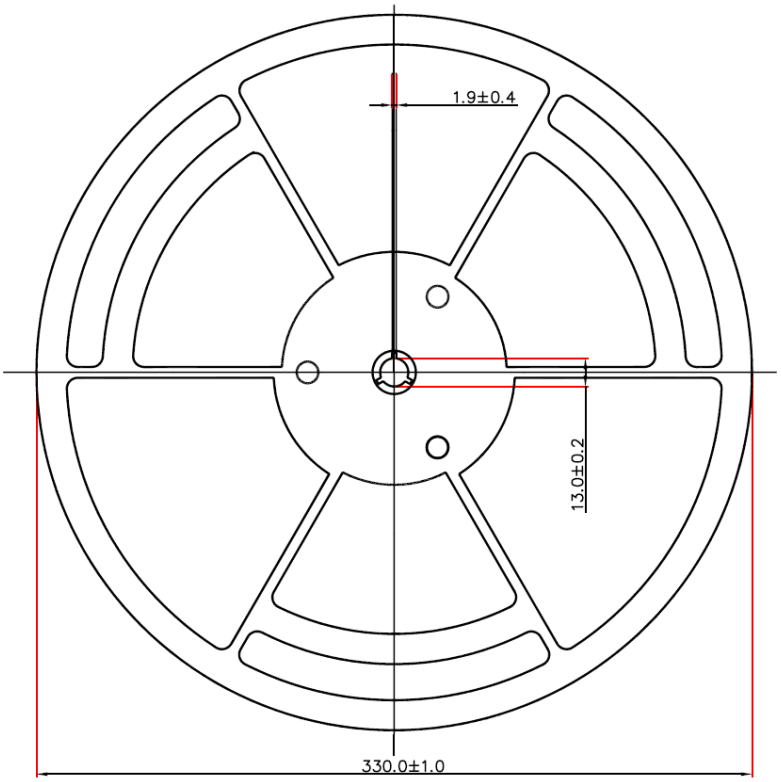


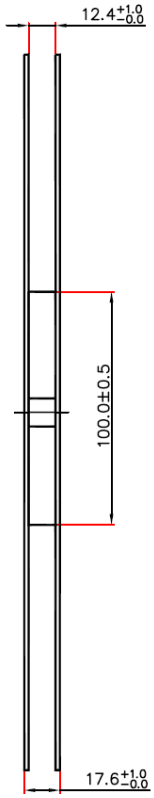


SECTION B–B



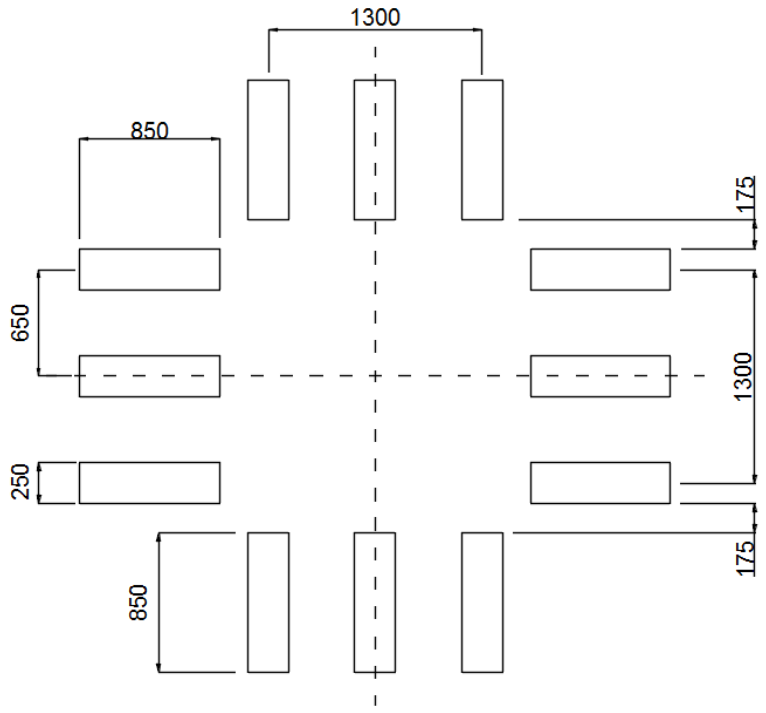
SECTION A–A





18. Recommended Land Pattern

FCQFN3X3-12L Package:



TOP VIEW

19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
INS2002FQ	FCQFN3x3-12L	2002FQ	MSL3	13” 2500PCS/reel

Important Notice

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