

INN80LA01

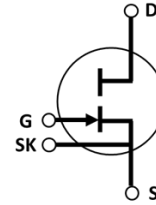
1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in LGA with 2.3 mm x 3.3 mm package size.

2. Features

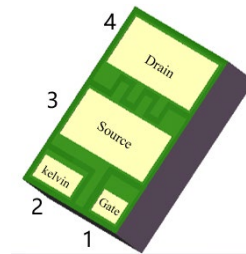
- AEC-Q101 Qualified*
- Ultra-High Switching Frequency and Ultra-Low $R_{DS(on)}$
- Fast and Controllable Fall and Rise Time
- Zero Reverse Recovery Loss

Note *: $V_{GS(TH)}$ shift ratio within 25% post 1000hrs reliability stress



3. Applications

- LiDAR Application
- Synchronous Rectification & Class-D Audio
- Envelope Tracking Power Supplies
- High Frequency DC-DC Converter



4. Key performance parameters

Table 1 Key performance parameters at $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS, max}$	80	V
$R_{DS(on), max}$ @ $V_{GS} = 5\text{ V}$	8	m Ω
Q_G, typ @ $V_{DS} = 40\text{ V}$	6.5	nC
$I_D, Pulse$	180	A
Q_{OSS} @40V	27.9	nC

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
1	Gate	Driver Gate
2	Kelvin	Kelvin Source
3	Source	Source
4	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN80LA01	LGA 2.3x3.3	G02

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6. Maximum ratings

at $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
V_{GS}	Gate-to-Source Forward Voltage	5.5	V
	Gate-to-Source Reverse Voltage	-4	V
I_D	Continuous Drain current	13	A
$I_{D, Pulse}$	Pulsed Drain Current (25°C , $T_{Pulse} = 100\text{ ns}$)	180	A
P_{tot}	Power dissipation	14	w
T_J	Operating Temperature	-40 to 125	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 to 150	$^\circ\text{C}$

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	38.6	°C/W	-
$R_{\theta JB}$	Thermal Resistance, Junction to Board	7	°C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ¹	36.3	°C/W	-
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise.

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	80	-	-	V	$V_{GS} = 0\text{ V}$, $I_D = 200\text{ }\mu\text{A}$
I_{DSS}	Drain-Source Leakage	-	24	144	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$
I_{GSS}	Gate-to-Source Forward Leakage	-	5	50	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Reverse Leakage	-	30	250	μA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}^1$	Gate Threshold Voltage	0.9	1.15	1.7	V	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$
$R_{DS(on)}$	Drain-Source On Resistance	-	6	8	$\text{m}\Omega$	$V_{GS} = 5\text{ V}$, $I_D = 10\text{ A}$

Note 1: $V_{GS(TH)}$ tested after I_{DSS} @ $V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$.

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{ISS}	Input Capacitance	-	750	1200	pF	V _{GS} = 0 V, V _{DS} = 40 V
C _{OSS}	Output Capacitance	-	330	450		V _{GS} = 0 V, V _{DS} = 40 V
C _{RSS}	Reverse Transfer Capacitance	-	8.2	15		V _{GS} = 0 V, V _{DS} = 40 V
		-	15.8	30		V _{GS} = 0 V, V _{DS} = 20 V
C _{OSS(ER)}	Energy Related C _{OSS}	-	538	-		V _{GS} = 0 V, V _{DS} = 0 to 40 V
C _{OSS(TR)}	Time Related C _{OSS}	-	697	-		V _{GS} = 0 V, V _{DS} = 0 to 40 V
Q _G	Total Gate Charge	-	6.5	8	nC	V _{GS} = 5 V, V _{DS} = 40 V, I _D = 10 A
Q _{GS}	Gate-to-Source Charge	-	1.2	-		V _{DS} = 40 V, I _D = 10 A
Q _{GD}	Gate-to-Drain Charge	-	1.1	-		V _{DS} = 40 V, I _D = 10 A
Q _{G(TH)}	Gate Charge at Threshold	-	0.8	-		V _{DS} = 40 V, I _D = 10 A
Q _{OSS}	Output Charge	-	27.9	-		V _{GS} = 0 V, V _{DS} = 40 V
R _G	Gate Resistance	-	1.5	3	Ω	f = 5 MHz, open drain

9. Electric characteristics diagrams

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise.

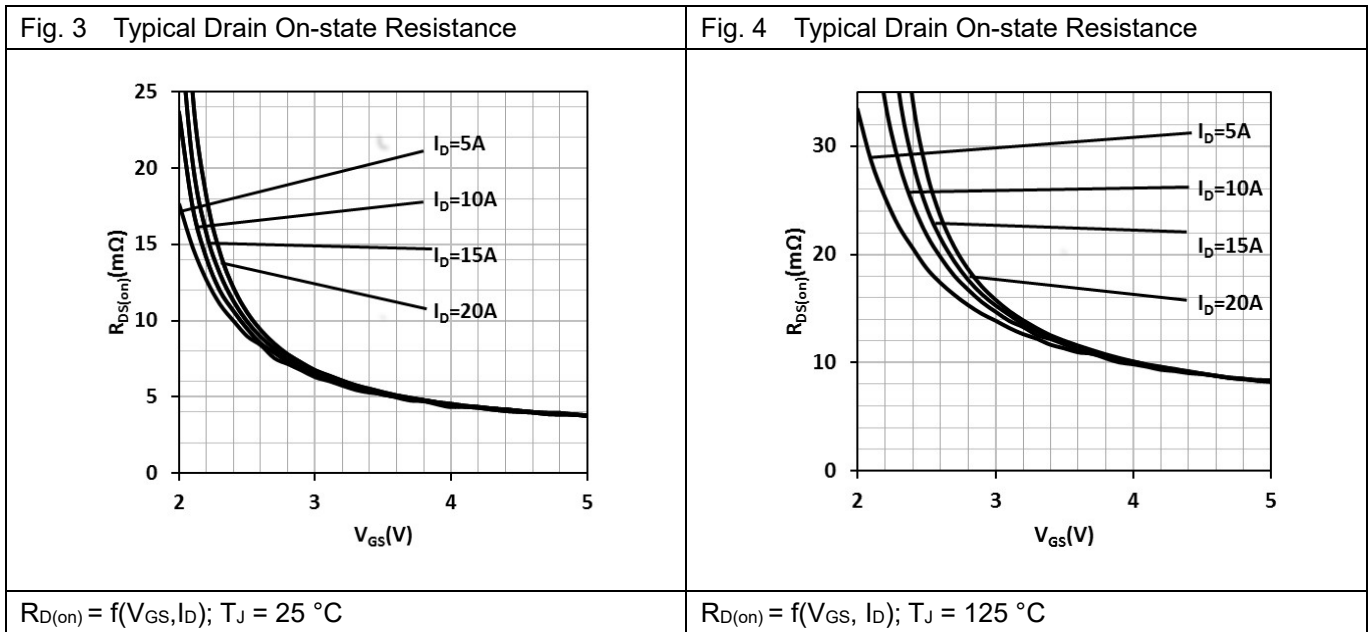
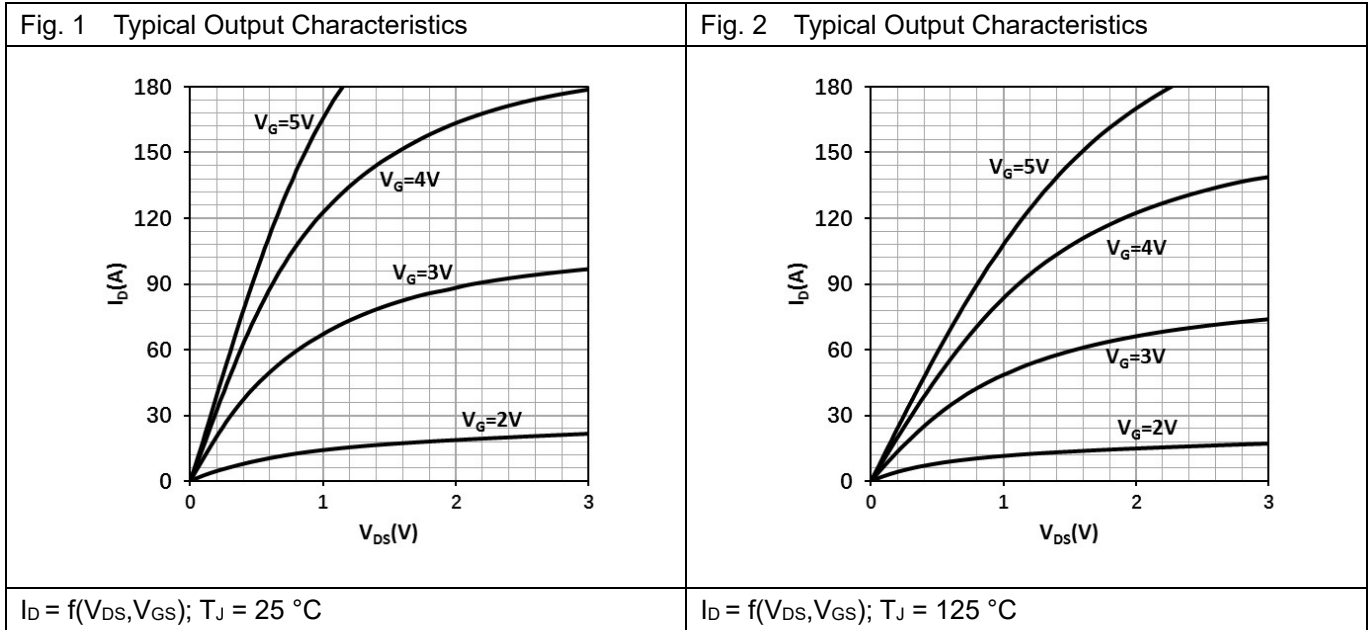
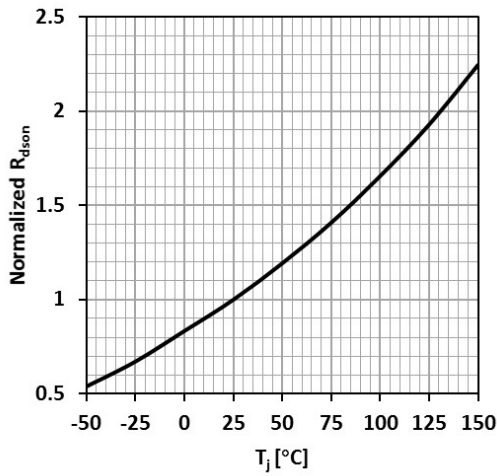
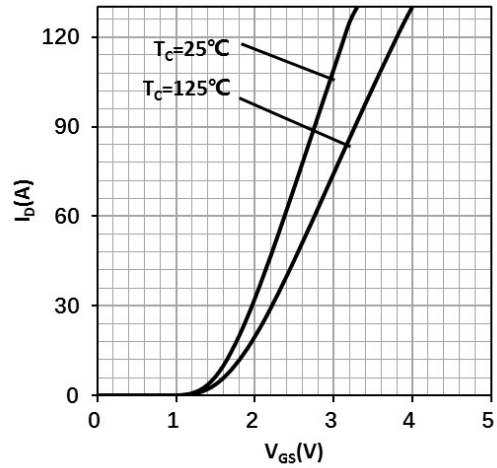


Fig. 5 Normalized On-State Resistance vs. Temp.



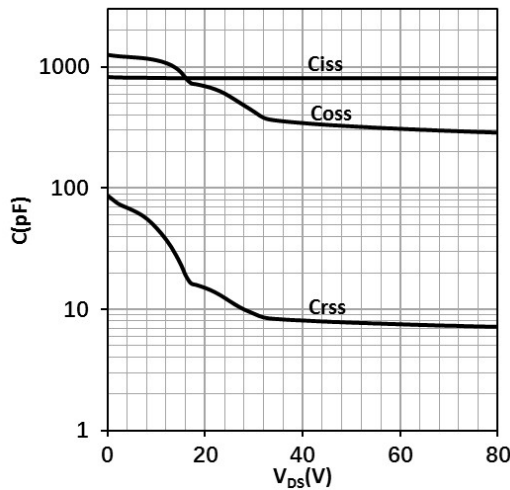
Normalized $R_{DS(on)} = f(T_J)$; $I_D = 10\text{ A}$

Fig. 6 Typical Transfer Characteristics



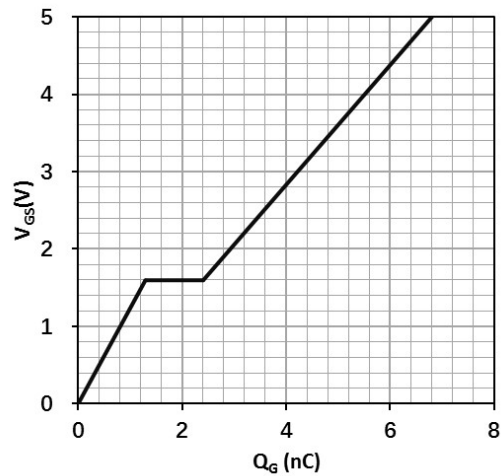
$I_D = f(V_{GS}, T_J)$; $V_{DS} = 3\text{ V}$

Fig. 7 Typ. Capacitances Characteristics



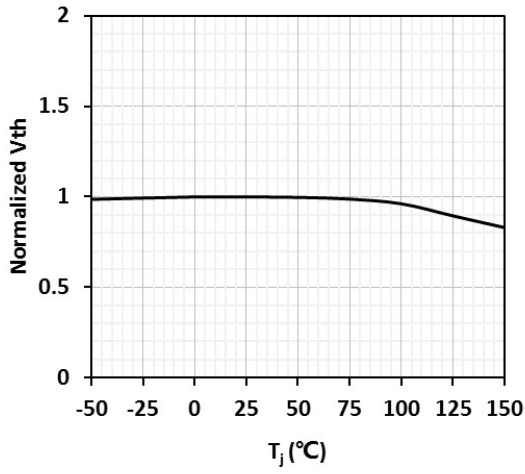
$C_{XSS} = f(V_{DS})$; $T_J = 25\text{ }^\circ\text{C}$

Fig. 8 Typ. Gate Charge



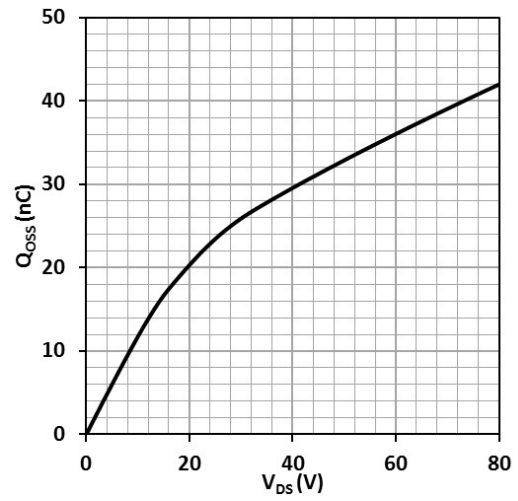
$V_{GS} = f(Q_G)$; $V_{DS} = 40\text{ V}$; $I_D = 10\text{ A}$

Fig. 9 Normalized Threshold Voltage vs. Temp.



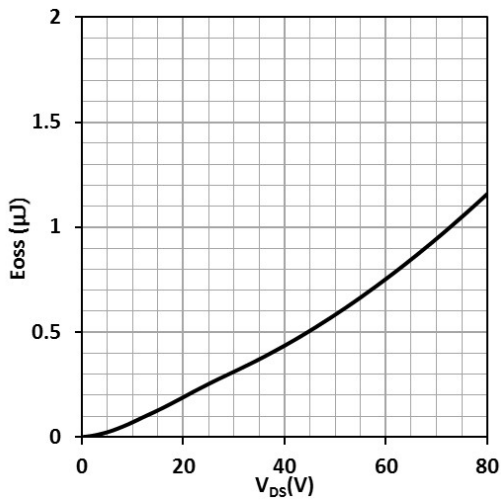
Normalized $V_{TH} = f(T_J)$; $V_{GS} = V_{DS}$; $I_D = 5 \text{ mA}$

Fig. 10 Output Charge



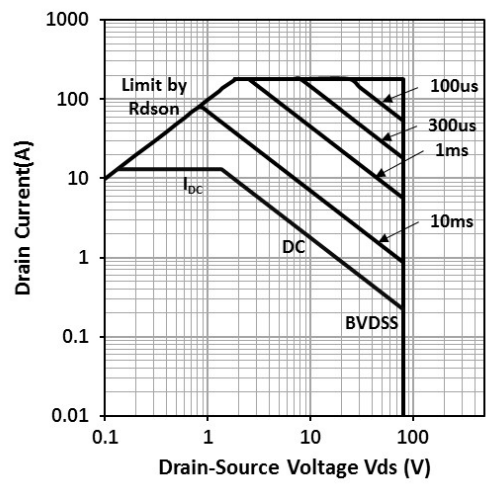
$Q_{oss} = f(V_{DS})$

Fig. 11 Output Capacitance Stored Energy



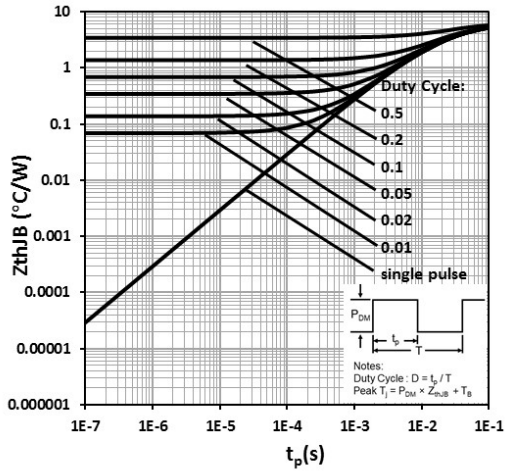
$E_{oss} = f(V_{DS})$

Fig. 12 Safe Operating Area



$I_D = f(V_{DS})$; $T_B = 25 \text{ }^\circ\text{C}$; Single Pulse

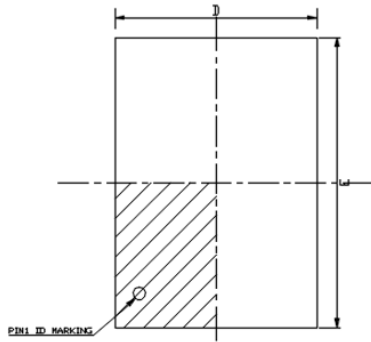
Fig. 13 Max. Transient Thermal Impedance



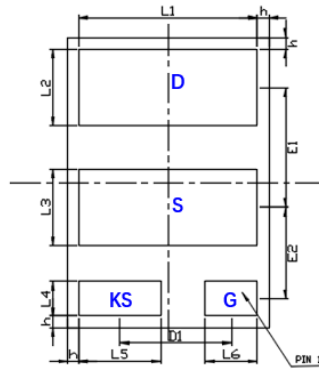
$Z_{\theta JB} = f(t_p);$

10. Package outlines

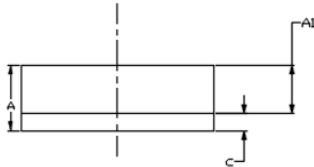
Package Reference



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.694	0.794	0.894
A1	0.58 BASIC		
c	0.184	0.214	0.244
D	2.20	2.30	2.40
D1	1.275 BASIC		
E	3.20	3.30	3.40
E1	1.37 BASIC		
E2	1.035 BASIC		
L1	1.990	2.040	2.090
L2	0.820	0.870	0.920
L3	0.820	0.870	0.920
L4	0.350	0.400	0.450
L5	0.880	0.930	0.980
L6	0.550	0.600	0.650
h	0.130 REF		

NOTE:

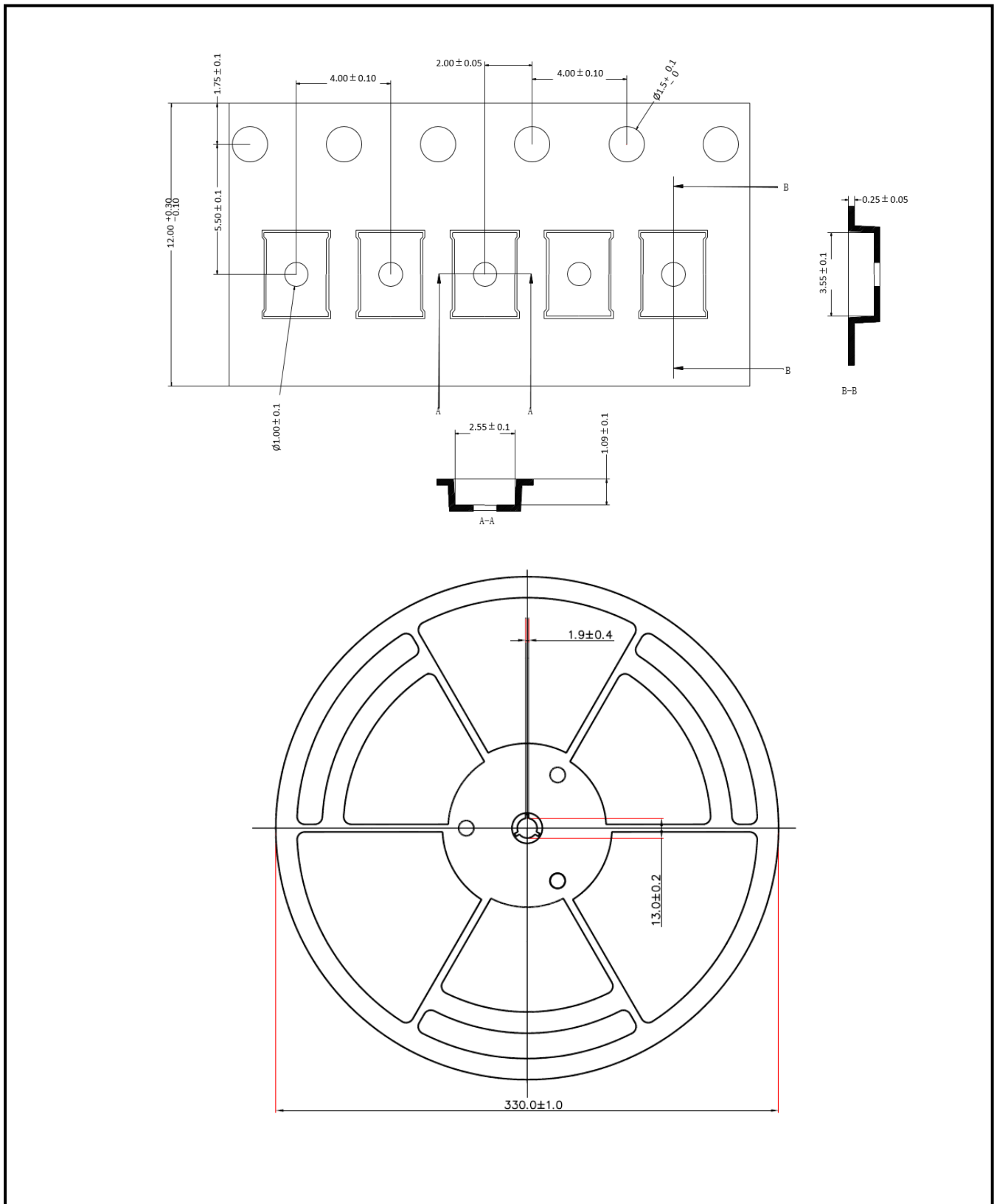
- 1) DIMENSION AND TOLERANCE CONFORM TO ASME Y14.5-2009
- 2) ALL DIMENSION ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) COMPLIES WITH JEDEC MO-303.
- 5) DRAWING IS NOT TO SCALE.

Marking Reference



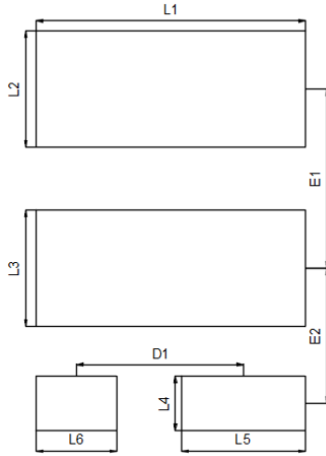
YYWW	Date Code
2D Code	1-3 Byte: Date Code
	4-9 Byte: Lot Number
	10-11 Byte: Strip Number
	12-15 Byte: Location ID in Strip

11. Reel information



12. Land Pattern

Recommended land pattern



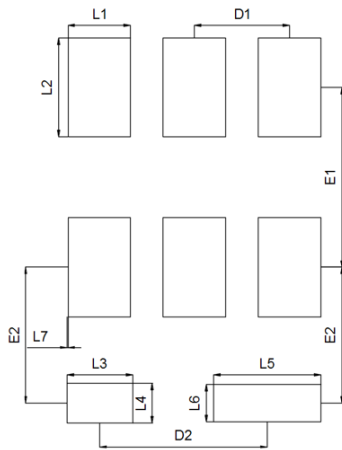
SYMBOL	MILLIMETER
	NOM
L1	2.060
L2	0.890
L3	0.890
L4	0.420
L5	0.950
L6	0.620
E1	1.370
E2	1.035
D1	1.275

TOP VIEW

NOTE:

- 1) LAND PATTERN IS SOLDER MASK DEFINED.
- 2) IT IS RECOMMENDED TO HAVE ON-CU TRACE PCB VIAS.

Recommended Stencil drawing



TOP VIEW

SYMBOL	MILLIMETER	NOTE
	NOM	
L1	0.475	6X
L2	0.755	6X
L3	0.500	
L4	0.300	
L5	0.815	
L6	0.285	
E1	1.370	3X
E2	1.035	2X
D1	0.725	4X
D2	1.275	
L7	0.075	

13. Revision history

Major changes since the last revision.

Revision	Date	Description of changes
1.0	2022-09-18	1.0 version setup
1.1	2023-03-01	1.1 update Package Reference & Land Pattern

Important Notice

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