INNEHB040A1
Evaluation Board Manual
40V GaN HEMT
Open Loop Half-Bridge EVB
CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by

⚠️ ELECTRICAL SHOCK HAZARD
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

⚠️ HOT SURFACE
The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

⚠️ REMINDER
This product contains parts that are susceptible to electrostatic discharge (ESD).
When using this product, be sure to follow antistatic procedures.
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1. Overview

1.1. Introduction

INNEHB040B1 is a half-bridge evaluation board equipped with uP1966E half-bridge gate driver to evaluate the performance of 40V GaN HEMT INNO40FQ043A. This board can simplify the test process, it can easily realize Buck or Boost converter with single or dual PWM input. The board includes all the necessary information you need, and the layout has been optimized to achieve the best performance. Test points are also included for the waveform measurement and efficiency evaluation.

1.2. Test Equipment Requirement

To evaluate the performance properly, you need to prepare the following test equipment:

1) High speed digital oscilloscope (>200MHz Bandwidth)
2) Low voltage DC power supply
3) PWM generator
4) Digital Multimeter
5) DC load (E-load or Power Resistor)
2. Parameters

<table>
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<tr>
<th>Symbol</th>
<th>Parameters</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
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<td>Gate Drive Regulator&lt;br&gt;Supp</td>
<td>7</td>
<td>12</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vin</td>
<td>Input Voltage</td>
<td></td>
<td>32&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Pout</td>
<td>Output Power</td>
<td></td>
<td>200&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td></td>
<td>W</td>
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<tr>
<td>Vpwm</td>
<td>Input Logic ‘High’</td>
<td>3.5</td>
<td>5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Input Logic ‘Low’</td>
<td>0</td>
<td>1.5</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 40 V for INN040FQ043A.

(2) Maximum output power depends on die temperature – actual maximum output power with be subject to switching frequency, bus voltage, load current and thermal cooling.
3. Block Diagram

Figure 1 INNEHB040B1 Block Diagram
4. PCBA Overview and Schematic

4.1. PCBA Overview

Figure 2 Top view of INNEHB040A1

Figure 3 Bottom view of INNEHB040A1
4.2. Schematic

![Schematic Diagram](image)

Figure 4 Schematic
5. Testing Guide

5.1. Test point location

![Diagram of measurement points]

Figure 5  Measurement points

5.2. Test setup

5.2.1. Buck Mode
Before tests, single or dual PWM input modes could be selected. When selecting the single PWM input mode, please solder 0Ω resistor to R9 & R13. The dead time is regulated by R11, R16, C1 and C2. The default value for R11...
and R16 is 300Ω, the value of C1 and C2 is 200 PF, and the corresponding dead interval is 20ns.

To select dual PWM mode, please solder 0Ω resistor to R10, R14, R11 and R16. Figure 7 Dual-PWM input Buck mode shows the required PWM signals; PWM1 and PWM2 should be complementary. The dead time is controlled by the signal generator.

5.2.2. Boost Mode

Figure 8 Single-PWM input Boost mode
5.3. Power up and down sequence

5.3.1. Power-up sequence (Buck Mode)

1. Check every power supply is off.

2. Connect the DC voltage source to VIN terminal P1 and common ground GND terminal P3, as shown in Figure 6 (Pay attention to the polarity).

3. Connect the electronic load to pin J1.

4. Connect the auxiliary source to the VDD terminal P4 (Pay attention to the polarity).

5. Connect the signal generator to pin P5.

6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.

7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.

8. Make sure the initial input supply voltage is 0 V, turn on the power and
slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switchnode and view the switching operation.

9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.2. Power-up sequence (Boost Mode)

1. Check every power supply is off

2. Connect the DC voltage source to pin J1, as shown in Figure 8 (Pay attention to the polarity).

3. Connect the positive pole of the electronic load to pin P1 and the negative pole to pin P3.

4. Connect the auxiliary source to the VDD terminal P4 (Pay attention to the polarity).

5. Connect the signal generator to pin P5.

6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.

7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.

8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switchnode and view the switching operation.

9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.3. Power-down sequence

1. Turn off the E-load first

2. Turn off the DC voltage source

3. Turn off the PWM generator

4. Turn off the auxiliary power supply
6. Evaluation Results

6.1.1. Switching Waveforms (Rgon=0Ω, Rgoff=0Ω)

**Test conditions**
- Vin=20Vdc
- Vout=12Vdc
- Iout=16A
- fsw=800kHz
- No Airflow

**Results**
- Vgs max: 5.145V
- Vsw overshoot: 11.76V
- Vgs rising time: 3.167ns
- Vgs falling time: 2.554ns
- Vds rising time: 1.520ns
- Vds falling time: 1.473ns

6.1.2. Efficiency Results

**Test conditions**
- Vin=20Vdc
- Vout=12Vdc
- Iout=16A
- fsw=800kHz
- No Airflow
6.1.3. Thermal performance

<table>
<thead>
<tr>
<th>Test conditions</th>
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<tbody>
<tr>
<td>Buck Mode</td>
</tr>
<tr>
<td>Vin=20Vdc</td>
</tr>
<tr>
<td>Vout=12Vdc</td>
</tr>
<tr>
<td>Iout=16A</td>
</tr>
<tr>
<td>fsw=800kHz</td>
</tr>
<tr>
<td>L=2.4uH</td>
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<tr>
<td>No Airflow</td>
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</table>

<table>
<thead>
<tr>
<th>Result</th>
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<tbody>
<tr>
<td>Switching GaN:</td>
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<tr>
<td>117.0°C</td>
</tr>
<tr>
<td>Continuation GaN:</td>
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<tr>
<td>97.7°C</td>
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<tr>
<td>Inductor: 85.3°C</td>
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</table>
Appendix

Appendix A. PCB Layout

Figure 10 The top layer of INNEHB040A1

Figure 11 The first middle layer of INNEHB040A1
Figure 12 The second middle layer of INNEHB040A1

Figure 13 The bottom layer of INNEHB040A1
### Appendix B. BOM

<table>
<thead>
<tr>
<th>Designator</th>
<th>Part Number</th>
<th>Manufacture r</th>
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<tr>
<td>C1, C2</td>
<td>0402X201J500CT</td>
<td>Walsin</td>
<td>CAP, 200pF/50V, ±5%, C0G</td>
<td>C0603</td>
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<td>C3</td>
<td>TMIK1078B475KA-T</td>
<td>TAIYO YUDEN</td>
<td>CAP, 4.7uF/25V, ±10%, X7R</td>
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<td>C4, C6</td>
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<td>D3, D4</td>
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<td>Innoscience</td>
<td>GAN FETs, 40V/4.3mΩ,</td>
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<td>PANASONIC</td>
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<td>UNI-ROYAL</td>
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<td>U1</td>
<td>uP1966E</td>
<td>uPI Semiconductor</td>
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<td>U2</td>
<td>TPS70950DBVR-TP</td>
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