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POWER THE FUTURE

INNDD1K0A1

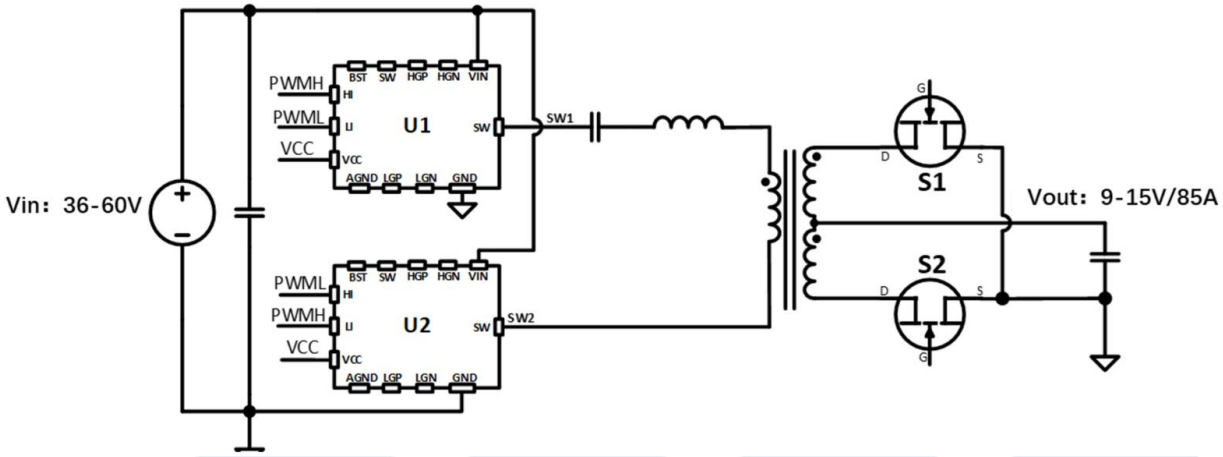
Demo Manual

1kW 48V/12V LLC DCX

1kW LLC DCX

Full Bridge LLC

Input voltage 36Vdc-60Vdc, output 9V-15V/85A, full-bridge open-loop LLC_DCX topology , fixed conversion ratio of 4:1 , maximum output power 1kW, switching frequency 1000 kHz, peak efficiency up to 98.0%.



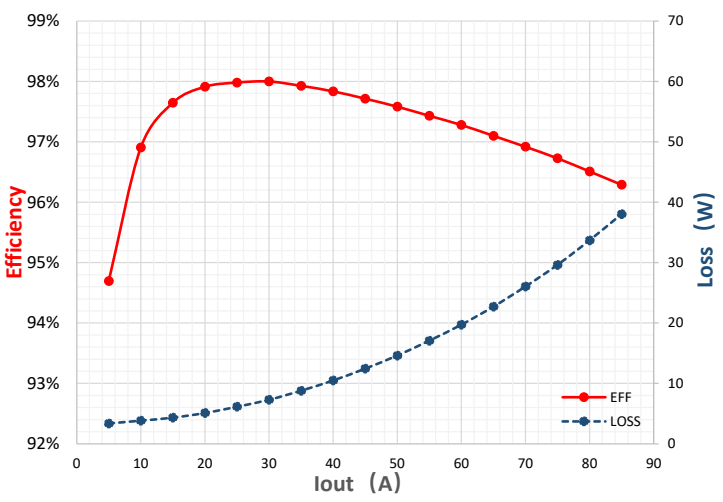
Highlighted Products

- U1/U2: ISG3201,
- S1/S2: INN040FQ015A

Target Applications

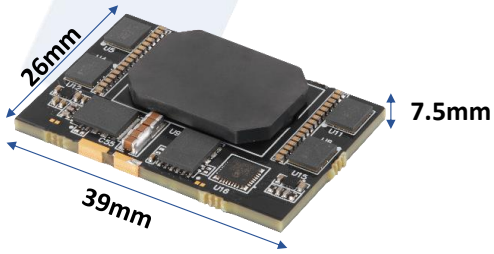
- Data Center
- Energy Storage
- Telecom

Test Results



Vin=48V, Vout=12V

Photo



List of Content

1. Overview

1.1. Description

INNDDD1K0A1 is a full-bridge open-loop LLC_DCX converter, input voltage 36Vdc-60Vdc, fixed conversion rate of 4:1, maximum output power 1kW, switching frequency 1000 kHz. It features the ISG3201 100V SolidGaN and INN040FQ015A enhancement mode field effect transistors.

1.2. Features

■ Main features and Advantages

- > High efficiency: 98.0% @48V to 12V delivering 30A output
- > High full-load efficiency: 96.29% @48V to 12V delivering 85A output
- > Fixed switching frequency: 1MHz
- > High power density: 2150W/in^3
- > Dimension: 39mm*26mm*7.5mm

1.3. Applications

- ■ Data Center
- ■ Energy Storage
- ■ Telecom

2. Parameters

Table 1 Electrical characteristics (Ta=25℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage			48	60	V
V_{OUT}	Output Voltage	Fixed ratio of 4:1 based on VIN		12		V
V_{AUX}	Auxiliary source voltage		7		12	V
P_{OUT}	Output Power				1000	W
f_s	Switching Frequency			1		MHz
	Cooling airflow			1900		LFM

3. Demo Solutions

3.1. System Solutions

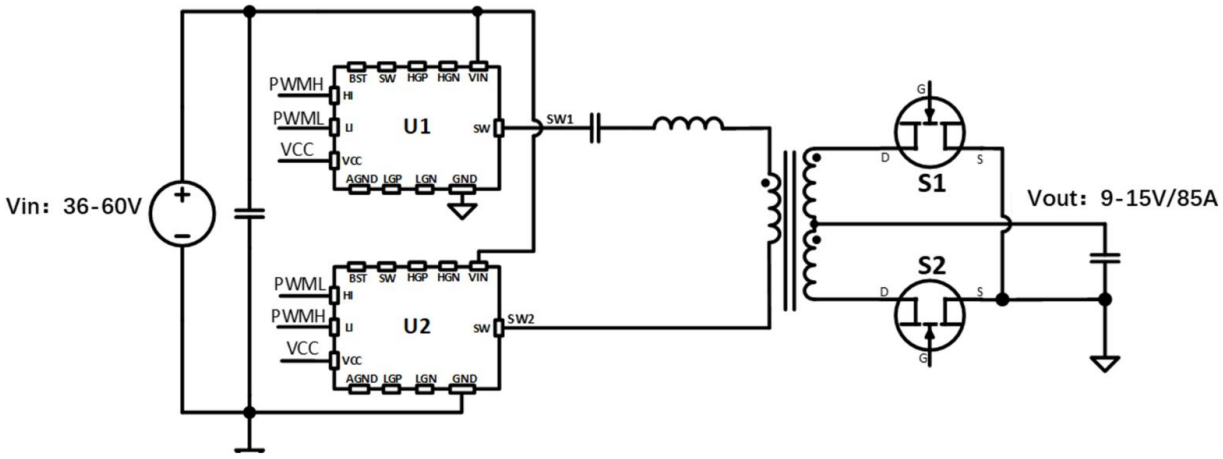


Figure 1 1kW LLC Demo board topology

The 1kW LLC demo board adopts the open-loop full-bridge LLC_DCX topology. Owing to the small capacitance parasitic junction of GaN, high efficiency and high power density are achieved.

3.2. Value of GaN

For soft switching applications, the switching loss ratio is very small due to the implementation of ZVS and ZCS. The key device parameters that affect the loss are output charge Qoss, gate charge Qg and drain-source on resistance.

■ Lower Qoss

The output charge Qoss of the device has a significant impact on the performance of resonant and soft switching converters, as it directly affects the energy required to achieve ZVS. The output charge Qoss of GaN is smaller, which means that the dead time required to achieve ZVS is smaller, and the RMS current of the resonator can be lower, resulting in higher system efficiency.

■ Lower Driver Losses

The gate charge Qg is the amount of charge required for a transistor to

be fully switched on or off. The gate charge Qg of GaN is smaller, which means that the driving loss is lower. In addition, the maximum switching frequency and switching speed are significantly affected by the gate charge Qg.

3.3. Highlighted Products

3.3.1. InnoGaN Device ISG3201

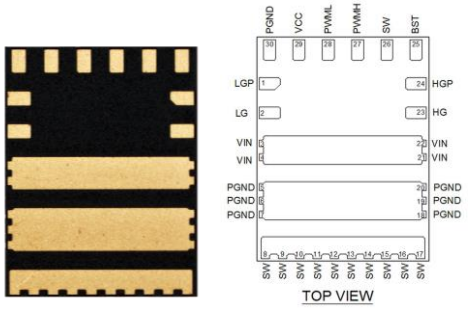


Figure 2 InnoGaN device ISG3201

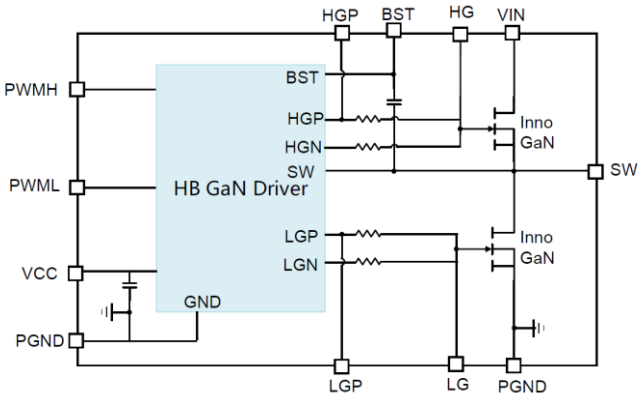


Figure 3 Block diagram of ISG3201

The ISG3201 is a 100V copak product in Innoscience's SolidGaN family. It integrates two 100V enhancement mode GaN devices with a 100V half-side diver voltage and can operate up to 100V. The integrated driver eliminates the external clamping circuit. Besides, turn-on and turn-off resistors, bootstrap and VCC decoupling caps are all integrated which makes the external circuit super simple. Due to excellent internal layout, the associated gate loop and power loop parasitic is reduced significantly, with value much less than 1nH. As a result, ultra-low voltage spike on switch nodes can be achieved. Turn-on speed of the half-bridge GaN HEMTs can be adjusted by an

optional single resister. The optimized pin layout of ISG3201 optimizes the power flow and simplifies the PCB board layout. ISG3201 employs independent high-side and low-side PWM input, which are usually available from most of GaN controllers. The ISG3201 is available in a compact 5mm× 6.5mm×1.08mm LGA package.

3.3.2. InnoGaN Device INN040FQ015A.

InnoGaN Device INN040FQ015A is a 40V enhancement mode high-electron-mobility-transistor(HEMT) in FCQFN with 5mm×4mm package size, with a maximum on resistance of 1.5mΩ. It features with ultra-low on resistance, very low gate charge, and zero reverse recovery charge.

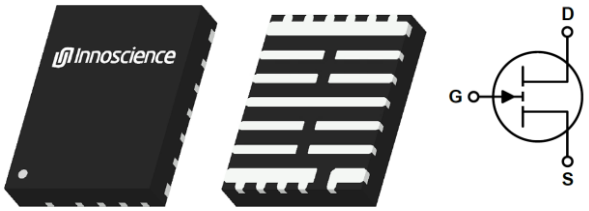


Figure 4 InnoGaN device INN040FQ015A

4. Hardware Implementation

4.1. Photos

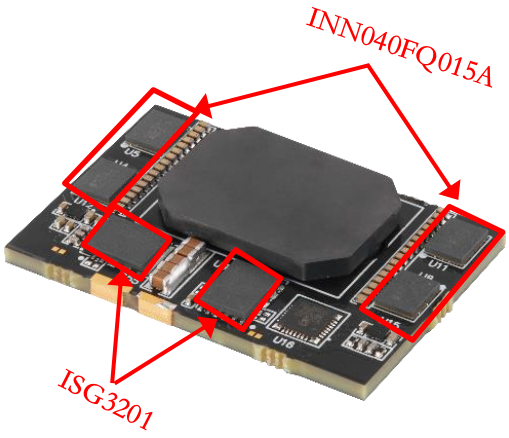


Figure 5 Top view of INNDDD1K0A1

4.2. Design Considerations

4.2.1. Magnetic Integrated Matrix Transformer

The transformer adopts the double magnetic column magnetic integration scheme with a turn ratio of 4:1:1. The UI-type magnetic core is embedded in the PCB to reduce the height of the product. The primary winding of transformer is connected in series and parallel, with each magnetic column winding two turns, and the two magnetic columns are connected in series to form four turns. The secondary winding adopts parallel mode, each magnetic column around one circle. The PCB has 14 layers in total. Considering that the current sharing of parallel layers is particularly important for overall efficiency, a symmetrical PCB winding arrangement with alternating MMF structure was adopted. The transformer adopts center-tapped rectifier structure, and there is a primary winding layer between every two secondary windings, forming a staggered structure, which greatly reduces the AC losses caused by eddy currents and proximity effects. The PCB winding stacking and alternating MMF structure diagram are shown in Figure6. Due to the open-loop LLC structure operating at a fixed frequency of 1MHz, the K value of the resonant cavity can be large, so the transformer leakage inductance can be

used as the resonant inductance, saving the volume of the external resonant inductance and achieving high power density.

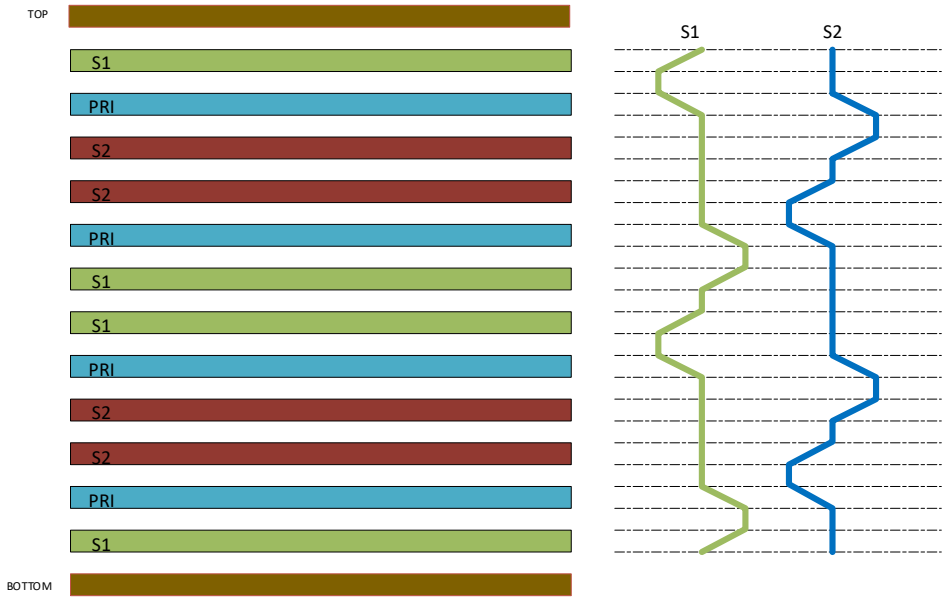


Figure 6 PCB winding stacking and magnetic potential schematic diagram

5. Testing & Results

5.1. Test Setup

The 1kW LLC demonstration board is easy to set up to evaluate the performance of ISG3201 100V SolidGaN and INN040FQ015A. Before the test, we need to get all the equipment prepared, which includes two DC sources, electronic load, digital multimeter, and digital oscilloscope with 1 GHz bandwidth. Refer to Figure7 and follow the procedure below for proper connection and measurement setup:

a) With power off, connect the input power supply to VIN to PGND as shown in Figure7.

b) With power off, connect the auxiliary source power supply to V_{AUX} to GND as shown in Figure7.

c) With power off, connect the load to V_{OUT} to SGND as shown in Figure7.

d) Turn on the auxiliary source power supply within 7V to 12V.

e) Turn on the input power supply at 0V and slowly increase the input voltage. Make sure that V_{IN} does not exceed 60V.

f) Once operational, adjust the load within the operating range and observe the efficiency, temperature and other characteristics. The maximum output power depends on the thermal state of the board, and the maximum operating temperature of the GaN transistor is required not to exceed the specification.

g) For shutdown, please follow the above steps in reverse.

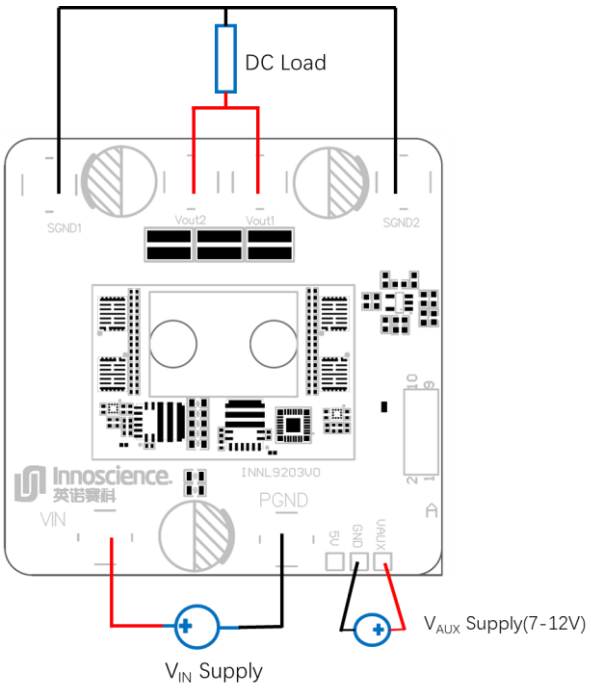


Figure 7 Proper Measurement Equipment Setup

5.2. Test Results

5.2.1. Efficiency curve

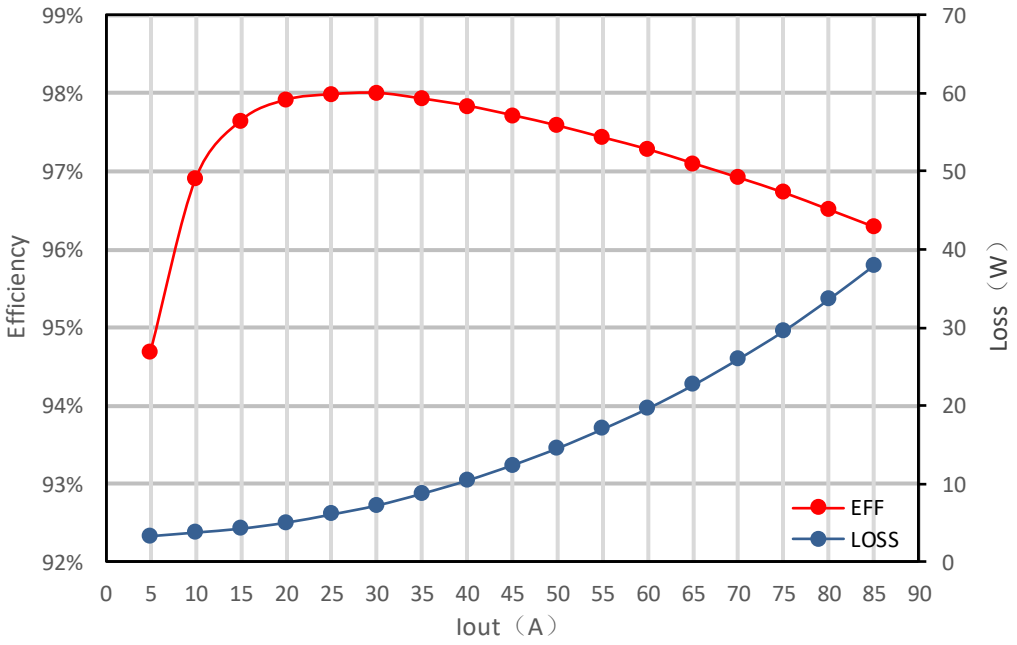


Figure 8 Efficiency Curve Vin=48V, Vo=12V, Fs=1000 kHz

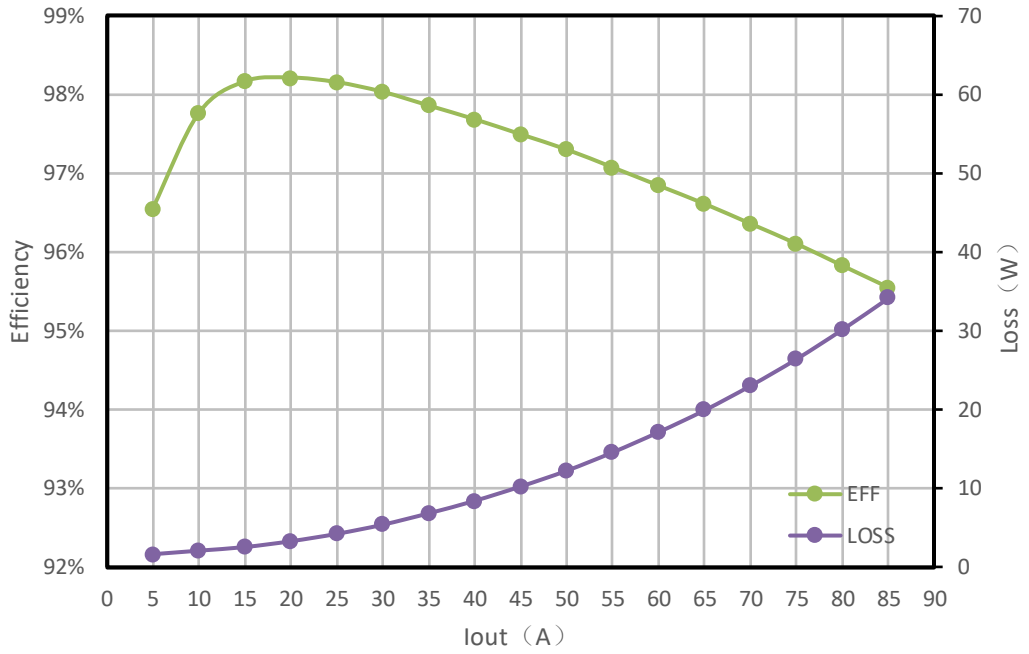


Figure 9 Efficiency Curve Vin=36V, Vo=9V, Fs=1000 kHz

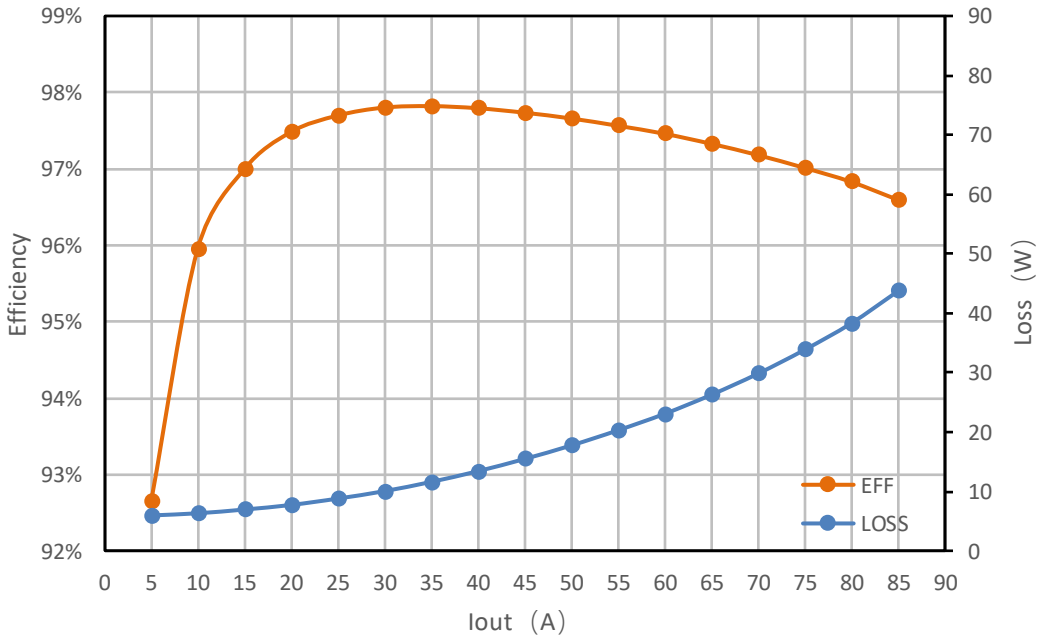
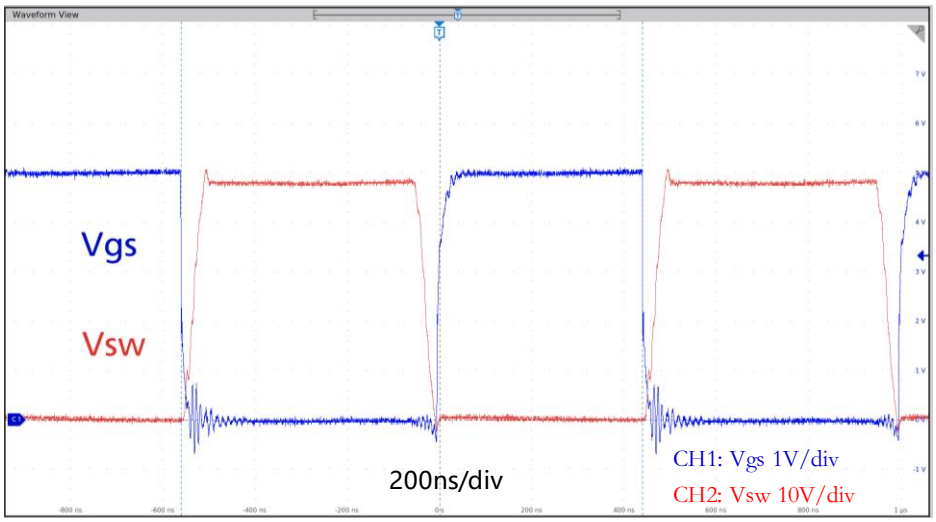


Figure 10 Efficiency Curve Vin=60V, Vo=15V, Fs=1000 kHz

5.2.2. Switching Waveforms



Test conditions

Vin: 48Vdc

Vo: 12V

Io: 85A

Fs: 1000 kHz

Test Result

SW Edge:

Rising Overshoot=2.6V

Rising time=34.5ns

Falling time=33.35ns

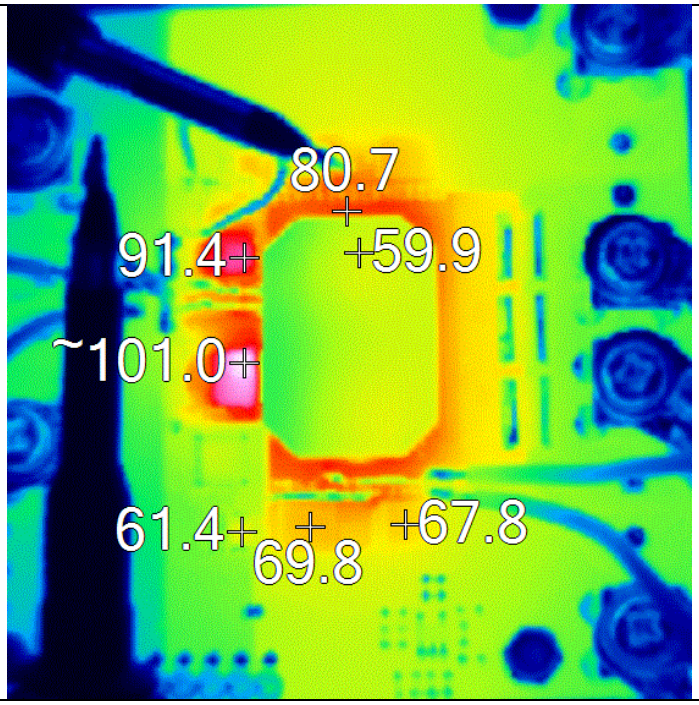
Falling Overshoot=-1.103V

U2_LG Edge:

Rising time=19.76ns,

Falling time=11.30ns

5.2.3. Thermal Test



Test conditions

Vin=48Vdc

Vout=12V

Iout=85A

Fs=1000 kHz

Ambient temp 25°C

Run for 0.5h

Result

Primary side SolidGan U1: 91.4℃

Primary side SolidGan U2: 101.0℃

Transformer: 59.9℃

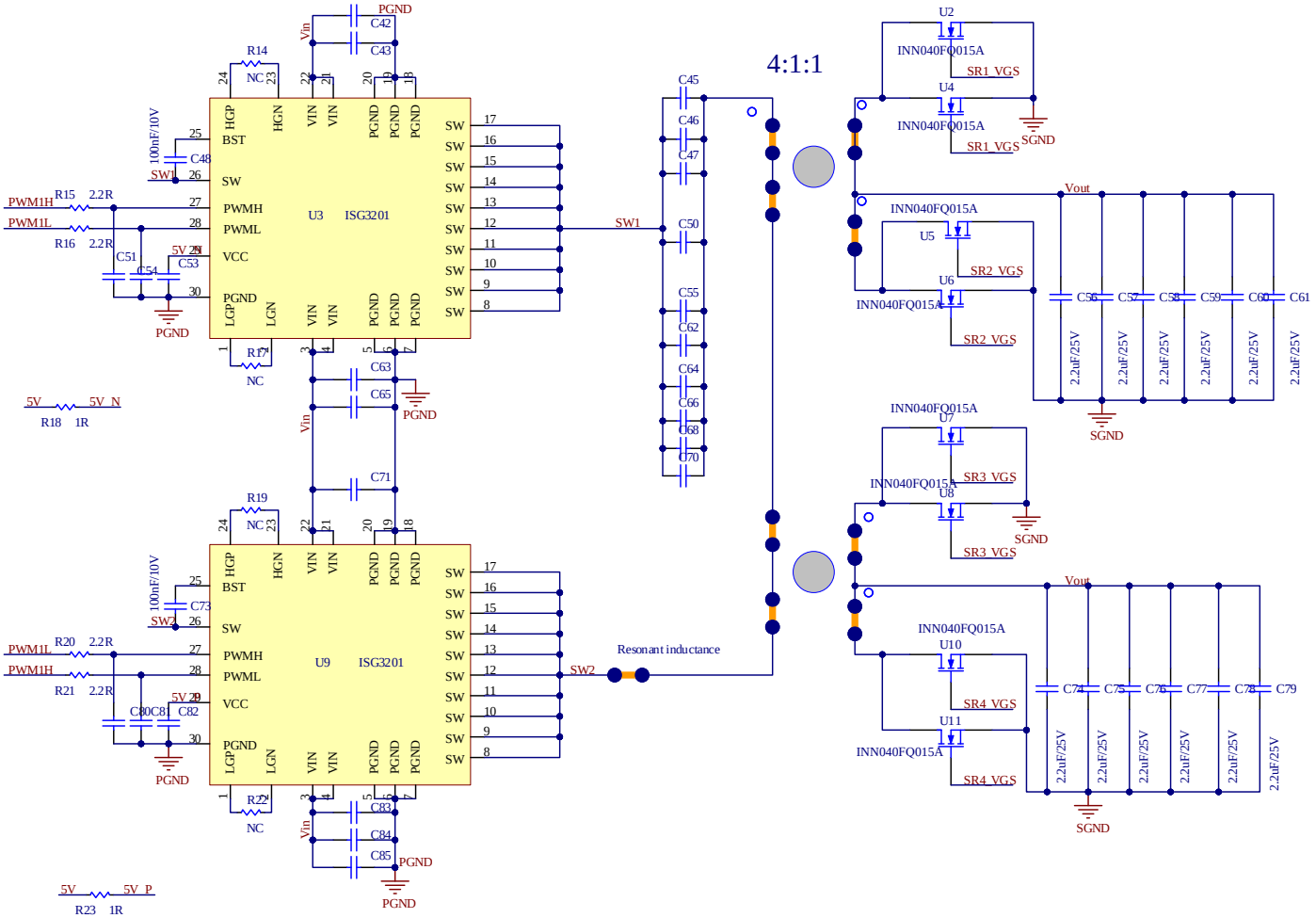
PCB Winding : 80.7 ℃

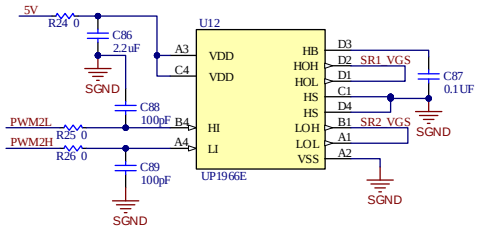
Secondary side GaN S1: 69.8℃

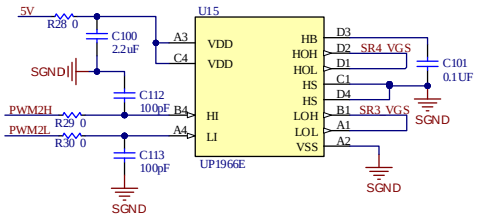
Secondary side GaN S2: 67.8℃

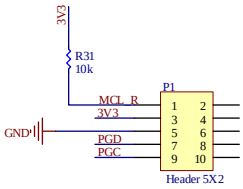
Appendix

Appendix A. Schematics

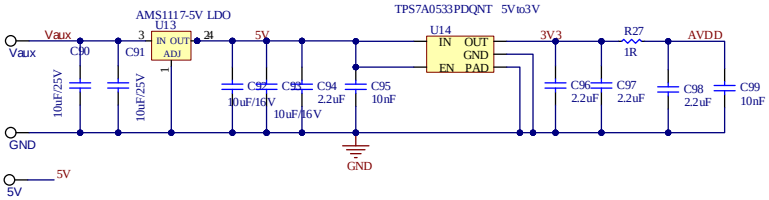


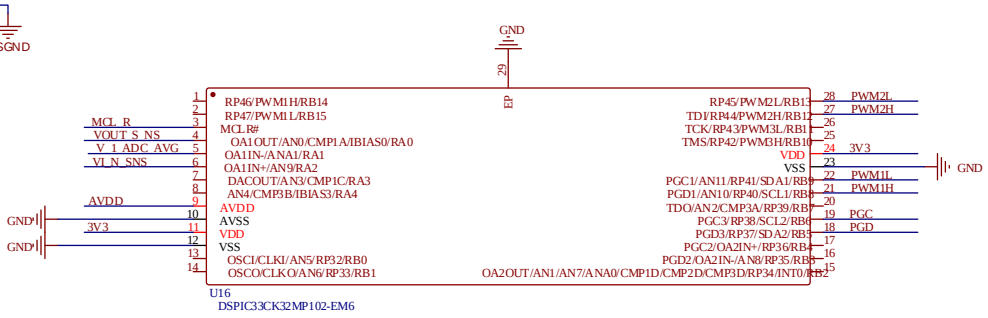






Auxiliary power supply





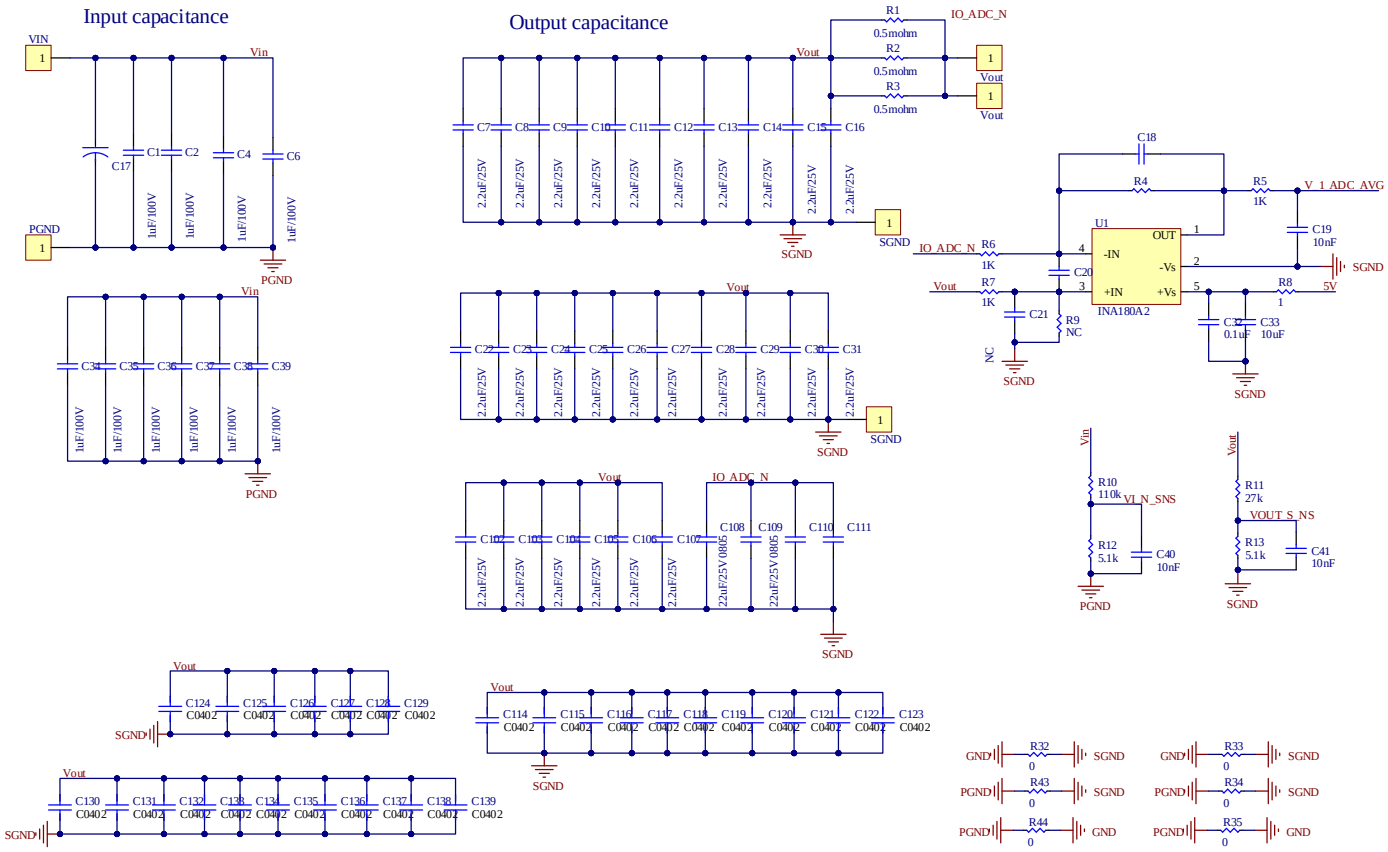


Figure 11 Schematic

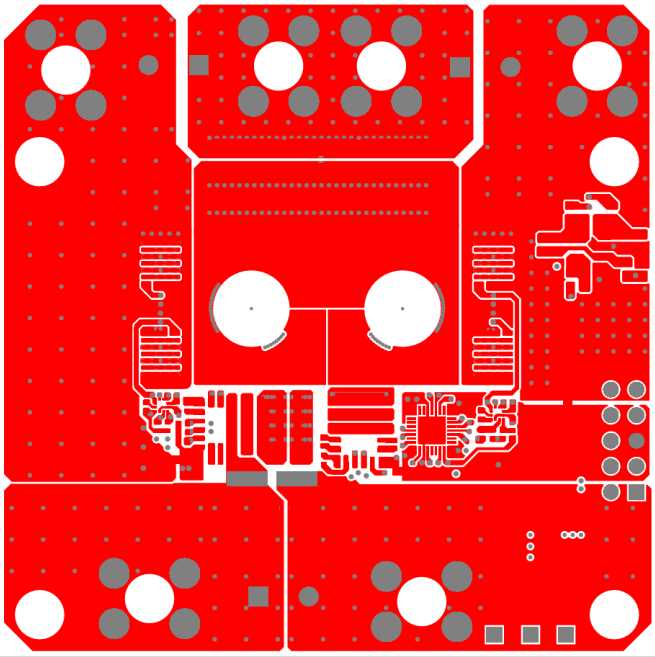
Appendix B. BOM

Table 2 BOM

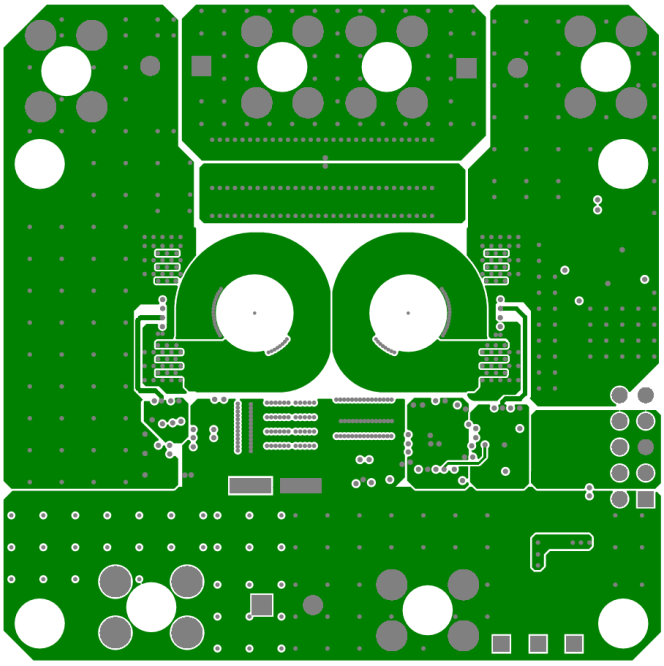
Designator	Comment	Description	Footprint	Quantity
C1, C2, C4, C6, C34, C35, C36, C37, C38, C39, C42, C43, C63, C65, C71, C83, C84, C85	Capacitor,1uF 0805 ±10% 100V X7S,	TDK,CGA4J3X7S2A105KT0Y0N	0805	18
C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C53, C56, C57, C58, C59, C60, C61, C74, C75, C76, C77, C78, C79, C82, C86,C94, C96, C97, C98, C100, C102, C103, C104, C105, C106, C107, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139,	Capacitor,2.2uF 0402 ±10% 25V X5R	muRata,GRM155R61E225KE11D	0402	72
C17	CE10, 100uF/100V	NC	EC10*12.5*5.0	1
C18	NC	NC	0603	1
C19, C40, C41	Capacitor,10nF/25V,±10% X7R	YAGEO,CC0603KRX7R8BB103	0603	3
C20	Capacitor,10pF/25V ±5% C0G	FH,0603CG100J250NT	0603	1
C21	Capacitor,200pF/50V ±5% NP0	YAGEO,CC0603JRNPO9BN201	0603	1
C32	Capacitor,0.1uF/25V ±10% X7R	YAGEO,CC0603KRX7R8BB104	0603	1
C33	Capacitor,10uF/25V,±10% X5R	muRata,GRM188R61E106KA73D	0603	1
C45, C46, C47, C50, C55,'C62, C64, C66, C68, C70	Capacitor,330nF/50V ±10% X7R	SAMSUNG,CL21B334KBFNNNE	0805	10
C48, C73,C87, C101	Capacitor,100nF/25V ±10% X5R	SAMSUNG,CL05A104KA5NNNC	0402	4
C51, C54, C80, C81, C88, C89, C112, C113	Capacitor,100pF/50V,±5% NP0	YAGEO,CC0402JRNPO9BN101	0402	8
C90, C91, C92, C93	Capacitor,10uF/25V,±10% X5R	SAMSUNG,CL21A106KAYNNNE	0805	4
C95, C99	Capacitor,10nF/16V,±10% X7R	YAGEO,CC0402KRX7R7BB103	0402	2
C108, C109	Capacitor,10uF/35V,±10% X5R	TAIYO YUDEN,GMK316BJ106KL-T	1206	2
C110, C111	Capacitor,100uF/50V	NC	EC10*12.5*5.0	2
P1	Header 5X2	Header, 5-Pin, Dual row	HDR2X5	1
R1, R2, R3	Chip resistors,0.5mohm,±5%	ROHM,PML100HZPJV0L5	R2512-FL	3
R4, R9	NC	NC	0603	2
R5,R6, R7	Chip resistors,1K±1%	YAGEO,RC0603FR-071KL	0603	3
R8	Chip resistors,1R±1%	YAGEO,RC0603FR-071RL	0603	1
R10	Chip resistors,110k±1%	PANASONIC,ERJ3EKF1103V	0603	1
R11	Chip resistors,27k±1%	UNI-ROYAL,0603WAF2702T5E	0603	1
R12, R13	Chip resistors,5.1k±1%	YAGEO,RC0603FR-075K1L	0603	2
R14, R17, R19, R22	NC	NC	0402	4
R15, R16, R20, R21	Chip resistors,2.2R±1%	UNI-ROYAL,0402WGF220KTCE	0402	4
R18, R23, R27	Chip resistors,1R,±1%	UNI-ROYAL,0402WGF100KTCE	0402	3
R24, R25, R26, R28, R29, R30	Chip resistors,0R,±1%	UNI-ROYAL,0402WGF0000TCE	0402	6
R31	Chip resistors,10k,±1%	YAGEO,RC0402FR-0710KL	0402	1

U1	Current-Sense Amplifiers	TI，INA180A2	SOT-23(5), 2.9mm*1.6 mm	1
U2, U4, U5, U6, U7, U8, U10, U11	GaN，40V/1.5mΩ	Innoscience，INN040FQ015A	FCQFN	8
U3, U9	SolidGaN, ISG3201	Innoscience，ISG3201	LGA 5mm*6.5m m	2
U12, U15	Dual-Channel Gate Driver	uPI SEMI, uP1966E	WLCSP 1.6*1.6-12B	2
U13	AMS1117-5V LDO	UMW, AMS1117-5V LDO	SOT223	1
U14	LDO，5Vto3.3V	TI，TPS7A0533PDQNT	X2SON （4） 1.0*1.0mm	1
U16	Digital signal controller	Microchip, DSPIC33CK32MP102-EM6	UQFN-28PIN	1
Magnetic core	ML91S L*W*h(21.6mm*15.4mm*7.0mm)	HITACHI, ML91S，		1

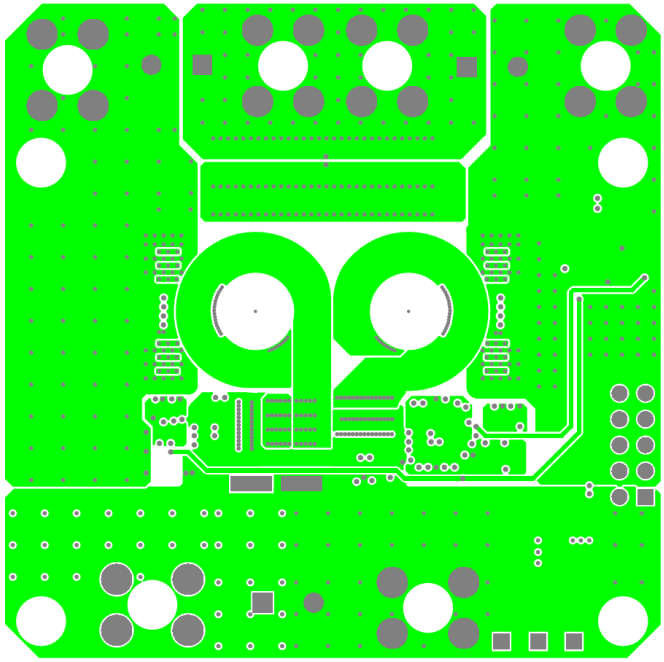
Appendix C. PCB Layouts



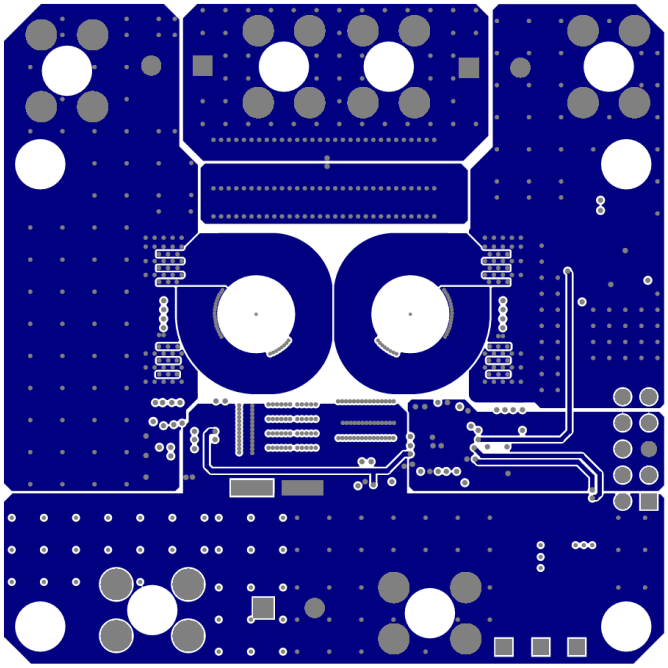
(a) Top Layer



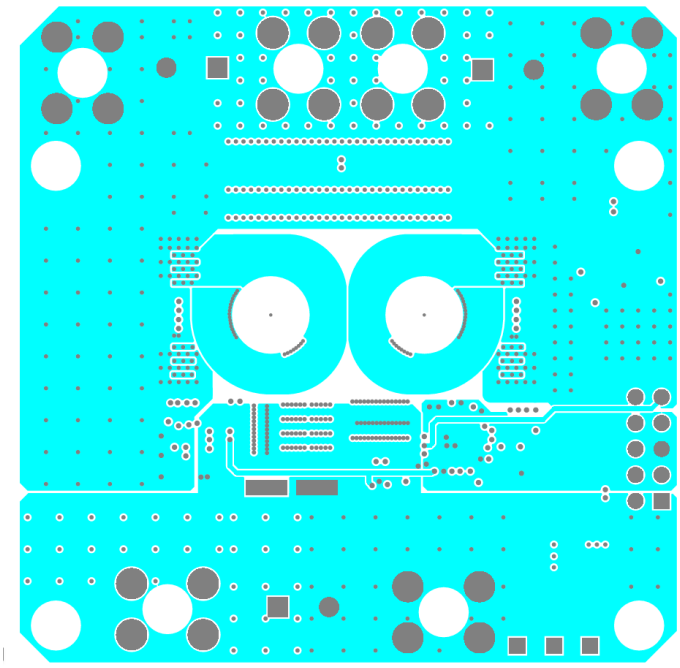
(b) Mid Layer 1



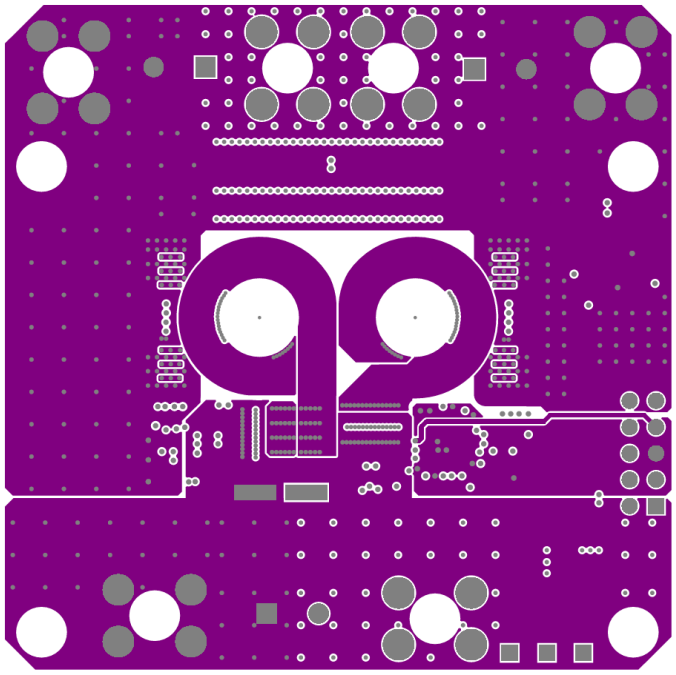
(c) Mid Layer 2



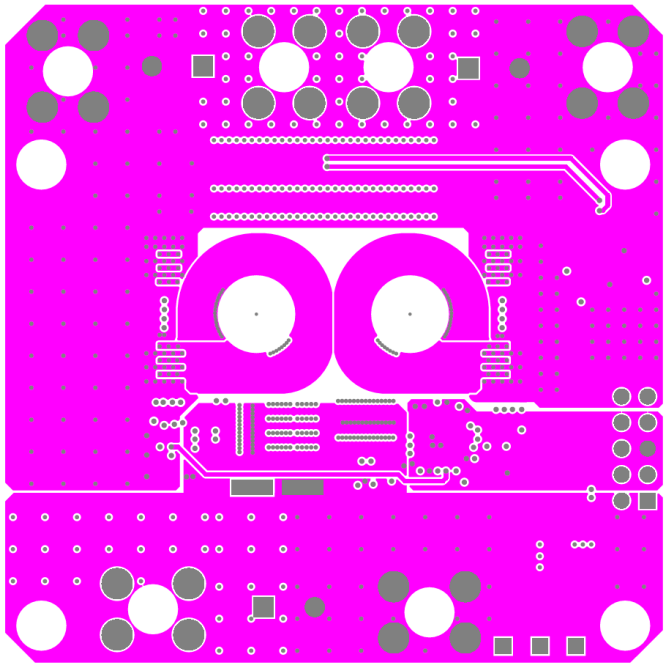
(d) Mid Layer 3



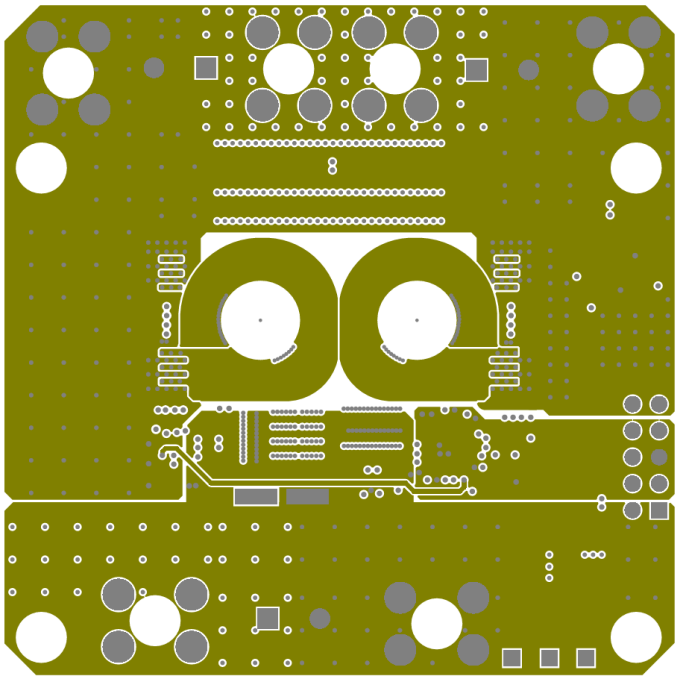
(e) Mid Layer 4



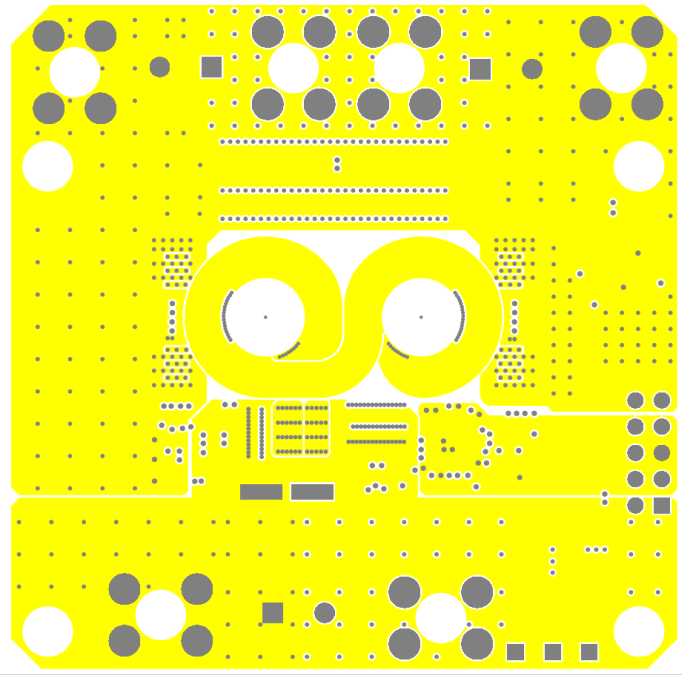
(f) Mid Layer 5



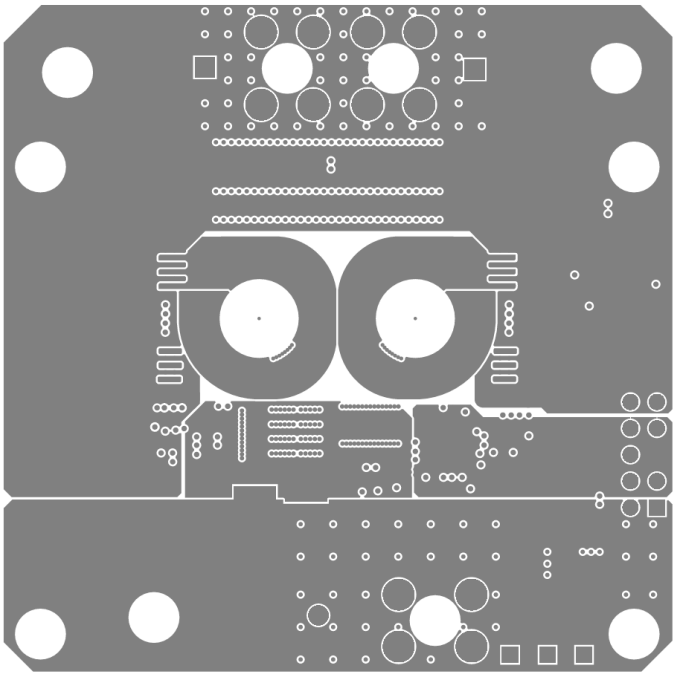
(g) Mid Layer 6



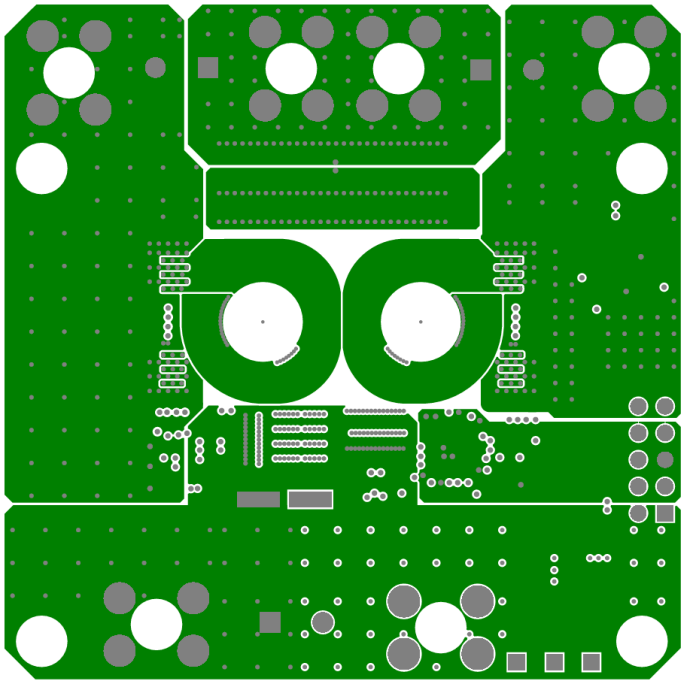
(h) Mid Layer 7



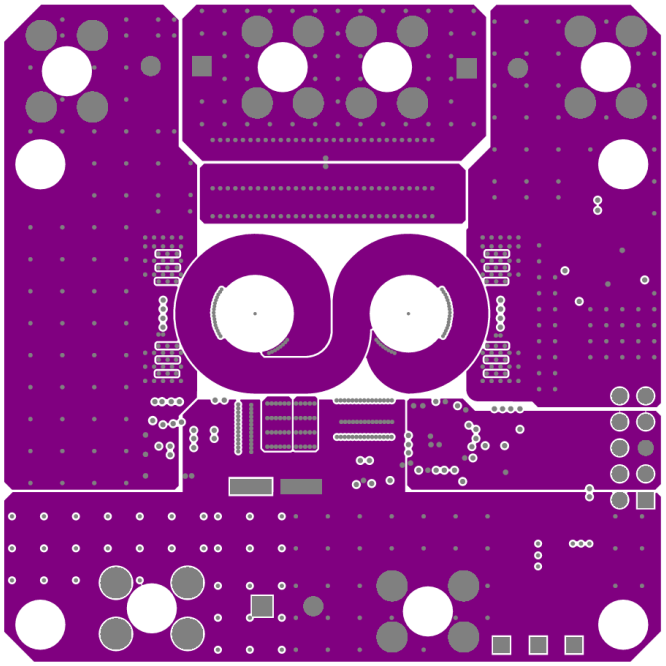
(i) Mid Layer 8



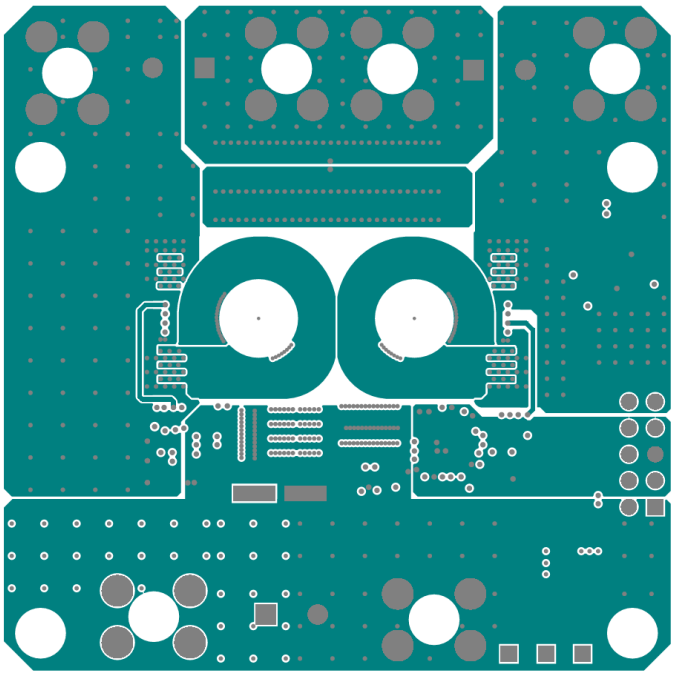
(j) Mid Layer 9



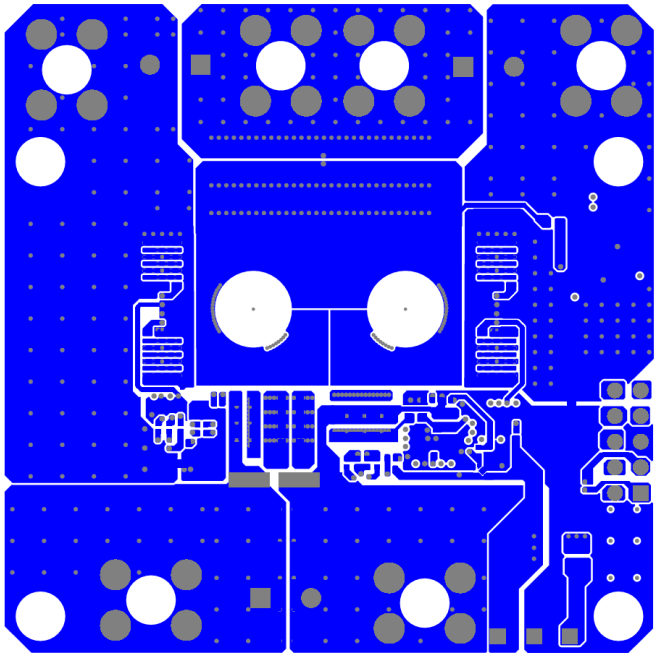
(k) Mid Layer 10



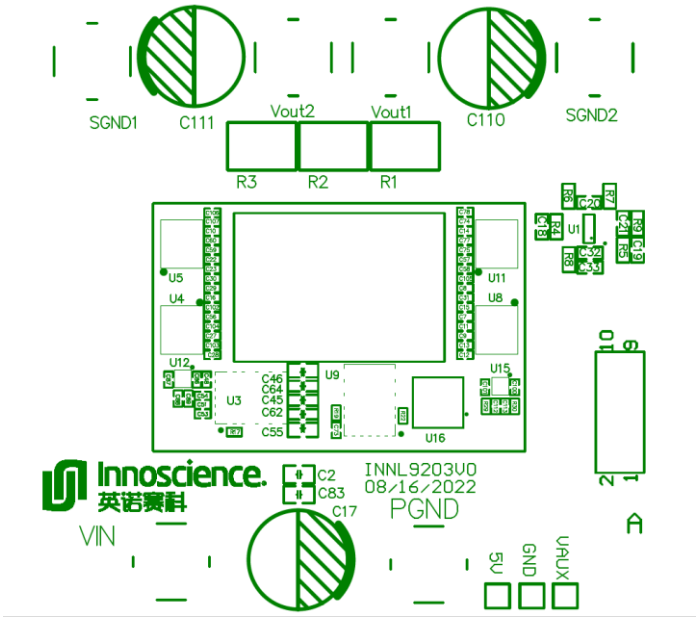
(l) Mid Layer 11



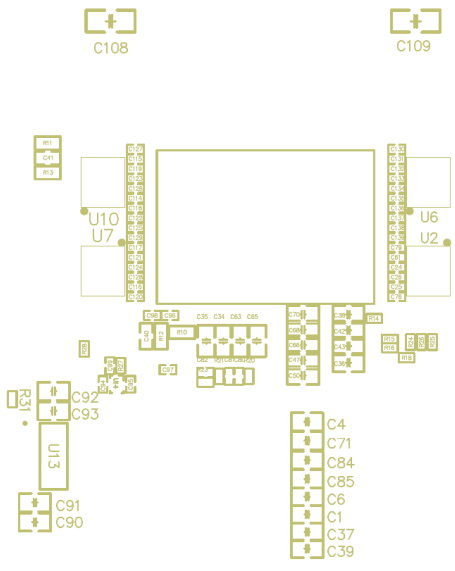
(m) Mid Layer 12



(n) Bottom Layer



(g) Top Overlayer



(h) Bottom Overlayer

Revision History

Date	Versions	Description	Author
2023/5/26	1.0	First edition	AE Team
2023/10/31	1.1	Update Part No.	AE Team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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